Wrap-Up

Part 1: Timing Analysis

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Simulation without SDF and without Testbench

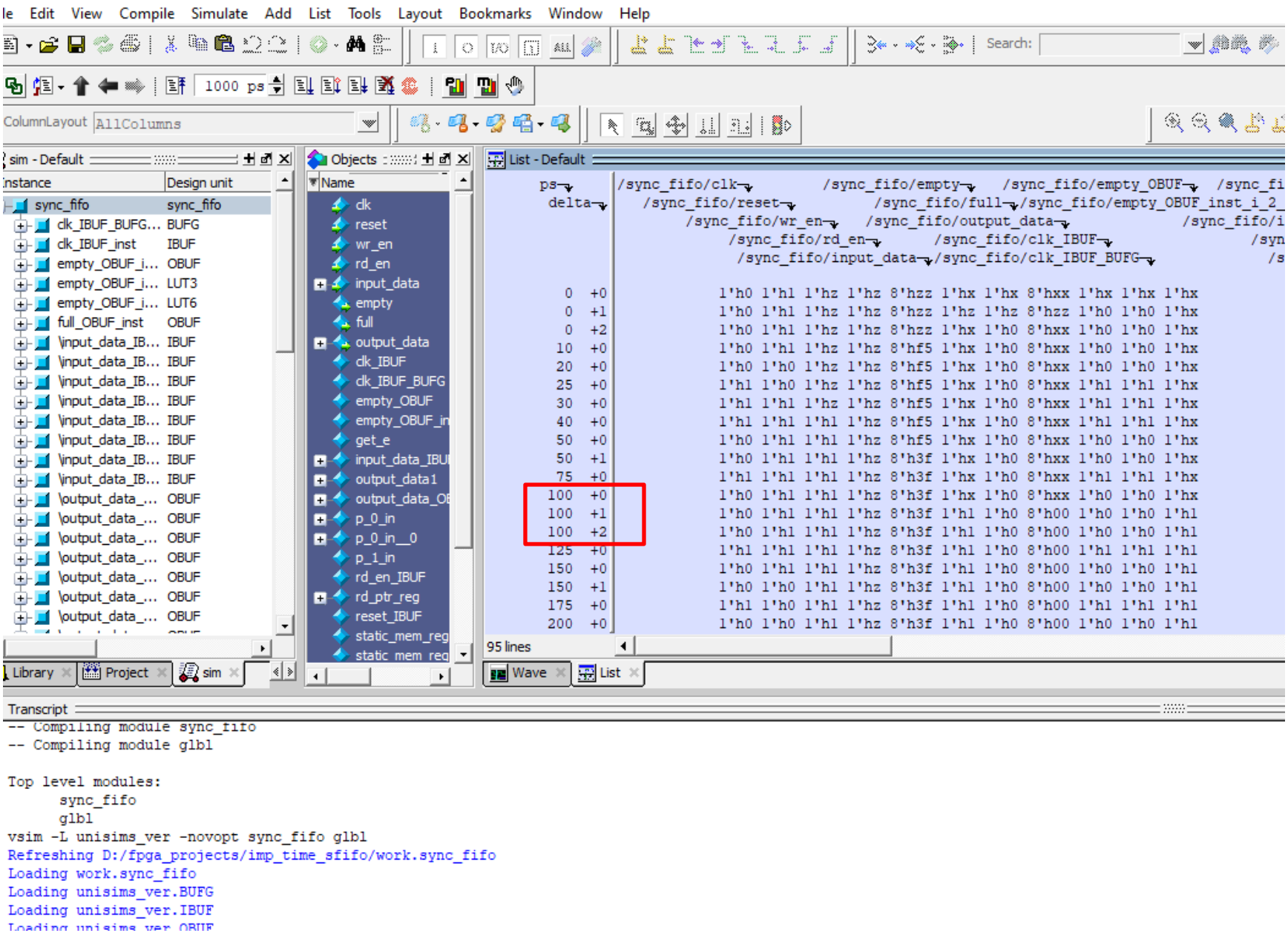
Questa

vsim -novopt sync_fifo -L unisims_ver glbl

```
Vivado% write_verilog -mode funcsim cnt16_netlist.v
```

```
vlib work
vmap work work
vlog sync_fifo_netlist.v
vsim -novopt sync_fifo -L unisims_ver glbl
add wave -r /*
add list -r /*

force -freeze clk 0 0, 1 {25 ps} -r 50
force reset 1
run 10
force input_data f5
run 10
force reset 0
run 10
force reset 1
run 10
force wr_en 1
run 10
force input_data 3f
run 100
force reset 0
run 300
force reset 1
force rd_en 1
run 400
force reset 0
run 200
```


Edit View Compile Simulate Add List Tools Layout Bookmarks Window Help
Search:
1000 ps
ColumnLayout AllColumns
sim - Default
Instance
Design unit
sync_fifo sync_fifo
clk_IBUF_BUFG... BUFG
clk_IBUF_inst IBUF
empty_OBUF_i... OBUF
empty_OBUF_i... LUT3
empty_OBUF_i... LUT6
full_OBUF_inst OBUF
\input_data_IB... IBUF
\output_data_... OBUF
Objects
Name
clk
reset
wr_en
rd_en
input_data
empty
full
output_data
clk_IBUF
clk_IBUF_BUFG
empty_OBUF
get_e
rd_en_IBUF
rd_ptr_reg
reset_IBUF
List - Default
ps
delta
/sync_fifo/clk
/sync_fifo/empty
/sync_fifo/empty_OBUF
/sync_fifo/reset
/sync_fifo/full
/sync_fifo/wr_en
/sync_fifo/output_data
/sync_fifo/rd_en
/sync_fifo/clk_IBUF
/sync_fifo/input_data
/sync_fifo/clk_IBUF_BUFG
0 +0 1'h0 1'hl 1'hz 1'hz 8'hzz 1'hx 1'hx 8'hxx 1'hx 1'hx 1'hx
0 +1 1'h0 1'hl 1'hz 1'hz 8'hzz 1'hz 1'hz 8'hzz 1'h0 1'h0 1'hx
0 +2 1'h0 1'hl 1'hz 1'hz 8'hzz 1'hx 1'h0 8'hxx 1'h0 1'h0 1'hx
10 +0 1'h0 1'hl 1'hz 1'hz 8'hf5 1'hx 1'h0 8'hxx 1'h0 1'h0 1'hx
20 +0 1'h0 1'h0 1'hz 1'hz 8'hf5 1'hx 1'h0 8'hxx 1'h0 1'h0 1'hx
25 +0 1'hl 1'h0 1'hz 1'hz 8'hf5 1'hx 1'h0 8'hxx 1'hl 1'hl 1'hx
30 +0 1'hl 1'hl 1'hz 1'hz 8'hf5 1'hx 1'h0 8'hxx 1'hl 1'hl 1'hx
40 +0 1'hl 1'hl 1'hl 1'hz 8'hf5 1'hx 1'h0 8'hxx 1'hl 1'hl 1'hx
50 +0 1'h0 1'hl 1'hl 1'hz 8'hf5 1'hx 1'h0 8'hxx 1'h0 1'h0 1'hx
50 +1 1'h0 1'hl 1'hl 1'hz 8'h3f 1'hx 1'h0 8'hxx 1'h0 1'h0 1'hx
75 +0 1'hl 1'hl 1'hl 1'hz 8'h3f 1'hx 1'h0 8'hxx 1'hl 1'hl 1'hx
100 +0 1'h0 1'hl 1'hl 1'hz 8'h3f 1'hx 1'h0 8'hxx 1'h0 1'h0 1'hx
100 +1 1'h0 1'hl 1'hl 1'hz 8'h3f 1'hl 1'h0 8'h00 1'h0 1'h0 1'hl
100 +2 1'h0 1'hl 1'hl 1'hz 8'h3f 1'hl 1'h0 8'h00 1'h0 1'h0 1'hl
125 +0 1'hl 1'hl 1'hl 1'hz 8'h3f 1'hl 1'h0 8'h00 1'hl 1'hl 1'hl
150 +0 1'h0 1'hl 1'hl 1'hz 8'h3f 1'hl 1'h0 8'h00 1'h0 1'h0 1'hl
150 +1 1'h0 1'h0 1'hl 1'hz 8'h3f 1'hl 1'h0 8'h00 1'h0 1'h0 1'hl
175 +0 1'hl 1'h0 1'hl 1'hz 8'h3f 1'hl 1'h0 8'h00 1'hl 1'hl 1'hl
200 +0 1'h0 1'h0 1'hl 1'hz 8'h3f 1'hl 1'h0 8'h00 1'h0 1'h0 1'hl
95 lines
Library
Project
sim
Wave
List
Transcript
-- Compiling module sync_fifo
-- Compiling module glbl
Top level modules:
sync_fifo
glbl
vsim -L unisims_ver -novopt sync_fifo glbl
Refreshing D:/fpga_projects/imp_time_sfifo/work.sync_fifo
Loading work.sync_fifo
Loading unisims_ver.BUFG
Loading unisims_ver.IBUF

Simulation with SDF and without Testbench

Questa

vsim -novopt sync_fifo -sdfmax postSynth.sdf -sdfnoerror -L simprims_ver glbl

- Note:

  postSynth.sdf -> full path to SDF file to apply delays only to netlist module

  -sdfmax -> optionally used with -sdfmin or –sdftyp

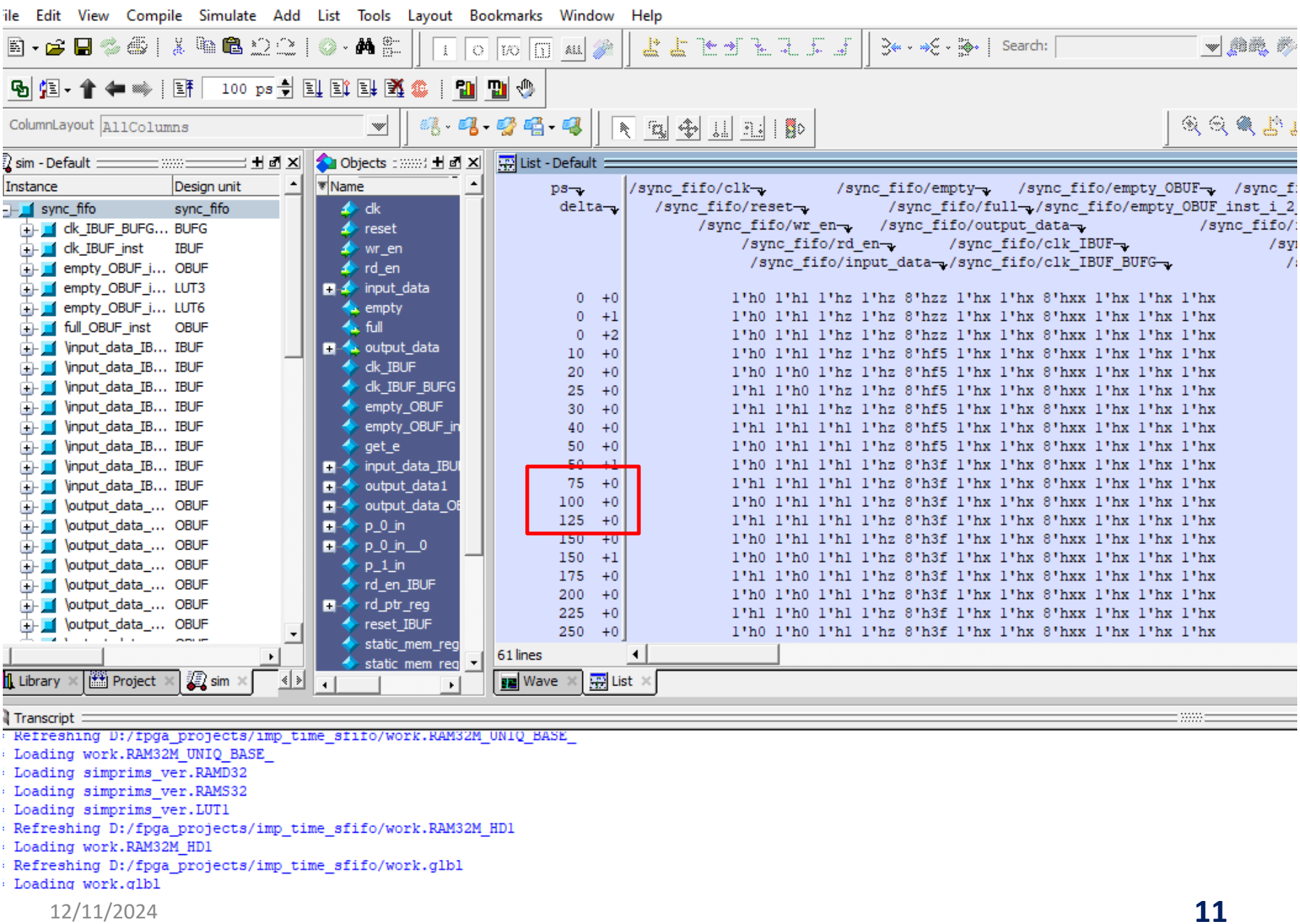
  -sdfnoerror -> reduce *SDF errors to warnings*, to enable simulation with missing hold times, etc.

  -L simprims_ver -> library of Verilog models only.

```
# Output Verilog netlist + SDC for timing simulation:
write_verilog -mode timesim -sdf_anno true postSynth_netlist.v
```

```
vlib work
vmap work work
vlog postSynth_netlist.v
vsim -novopt sync_fifo -sdfmax postSynth.sdf -sdfnoerror -L simprims_ver glbl
add wave -r /*
add list -r /*

force -freeze clk 0 0, 1 {25 ps} -r 50
force reset 1
run 10
force input_data f5
run 10
force reset 0
run 10
force reset 1
run 10
force wr_en 1
run 10
force input_data 3f
run 100
force reset 0
run 300
force reset 1
force rd_en 1
run 400
force reset 0
run 200
```


File Edit View Compile Simulate Add List Tools Layout Bookmarks Window Help
Search:
100 ps
ColumnLayout AllColumns
sim - Default
Instance
Design unit
sync_fifo
clk_IBUF_BUFG...
clk_IBUF_inst
empty_OBUF_i...
empty_OBUF_i...
empty_OBUF_i...
full_OBUF_inst
Objects
Name
clk
reset
wr_en
rd_en
input_data
empty
full
output_data
clk_IBUF
clk_IBUF_BUFG
empty_OBUF
get_e
p_0_in
p_0_in__0
p_1_in
rd_en_IBUF
rd_ptr_reg
reset_IBUF
List - Default
ps
delta
/sync_fifo/clk
/sync_fifo/reset
/sync_fifo/wr_en
/sync_fifo/rd_en
/sync_fifo/input_data
/sync_fifo/empty
/sync_fifo/full
/sync_fifo/output_data
/sync_fifo/clk_IBUF
/sync_fifo/clk_IBUF_BUFG
/sync_fifo/empty_OBUF
0 +0 l'h0 l'hl l'hz l'hz 8'hzz l'hx l'hx 8'hxx l'hx l'hx l'hx
0 +1 l'h0 l'hl l'hz l'hz 8'hzz l'hx l'hx 8'hxx l'hx l'hx l'hx
0 +2 l'h0 l'hl l'hz l'hz 8'hzz l'hx l'hx 8'hxx l'hx l'hx l'hx
10 +0 l'h0 l'hl l'hz l'hz 8'hf5 l'hx l'hx 8'hxx l'hx l'hx l'hx
20 +0 l'h0 l'h0 l'hz l'hz 8'hf5 l'hx l'hx 8'hxx l'hx l'hx l'hx
25 +0 l'hl l'h0 l'hz l'hz 8'hf5 l'hx l'hx 8'hxx l'hx l'hx l'hx
30 +0 l'hl l'hl l'hz l'hz 8'hf5 l'hx l'hx 8'hxx l'hx l'hx l'hx
40 +0 l'hl l'hl l'hl l'hz 8'hf5 l'hx l'hx 8'hxx l'hx l'hx l'hx
50 +0 l'h0 l'hl l'hl l'hz 8'hf5 l'hx l'hx 8'hxx l'hx l'hx l'hx
50 +1 l'h0 l'hl l'hl l'hz 8'h3f l'hx l'hx 8'hxx l'hx l'hx l'hx
75 +0 l'hl l'hl l'hl l'hz 8'h3f l'hx l'hx 8'hxx l'hx l'hx l'hx
100 +0 l'h0 l'hl l'hl l'hz 8'h3f l'hx l'hx 8'hxx l'hx l'hx l'hx
125 +0 l'hl l'hl l'hl l'hz 8'h3f l'hx l'hx 8'hxx l'hx l'hx l'hx
150 +0 l'h0 l'hl l'hl l'hz 8'h3f l'hx l'hx 8'hxx l'hx l'hx l'hx
150 +1 l'h0 l'h0 l'hl l'hz 8'h3f l'hx l'hx 8'hxx l'hx l'hx l'hx
175 +0 l'hl l'h0 l'hl l'hz 8'h3f l'hx l'hx 8'hxx l'hx l'hx l'hx
200 +0 l'h0 l'h0 l'hl l'hz 8'h3f l'hx l'hx 8'hxx l'hx l'hx l'hx
225 +0 l'hl l'h0 l'hl l'hz 8'h3f l'hx l'hx 8'hxx l'hx l'hx l'hx
250 +0 l'h0 l'h0 l'hl l'hz 8'h3f l'hx l'hx 8'hxx l'hx l'hx l'hx
61 lines
Library
Project
sim
Wave
List
Transcript
Refreshing D:/fpga_projects/imp_time_sfifo/work.RAM32M_UNIQ_BASE_
Loading work.RAM32M_UNIQ_BASE_
Loading simprims_ver.RAMD32
Loading simprims_ver.RAMS32
Loading simprims_ver.LUT1
Refreshing D:/fpga_projects/imp_time_sfifo/work.RAM32M_HD1
Loading work.RAM32M_HD1
Refreshing D:/fpga_projects/imp_time_sfifo/work.glbl
Loading work.glbl

Simulation with SDF and Testbench

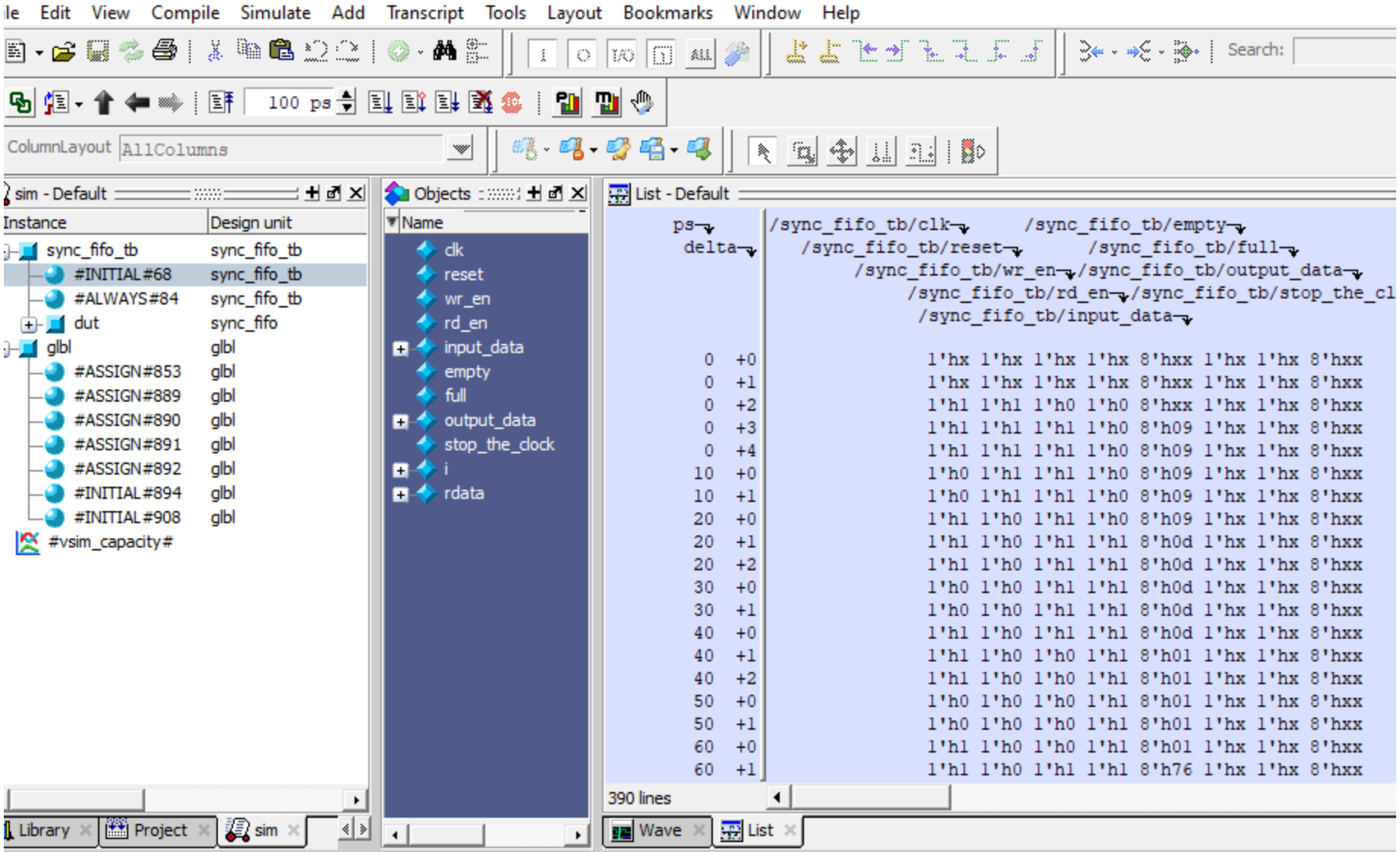
Questa

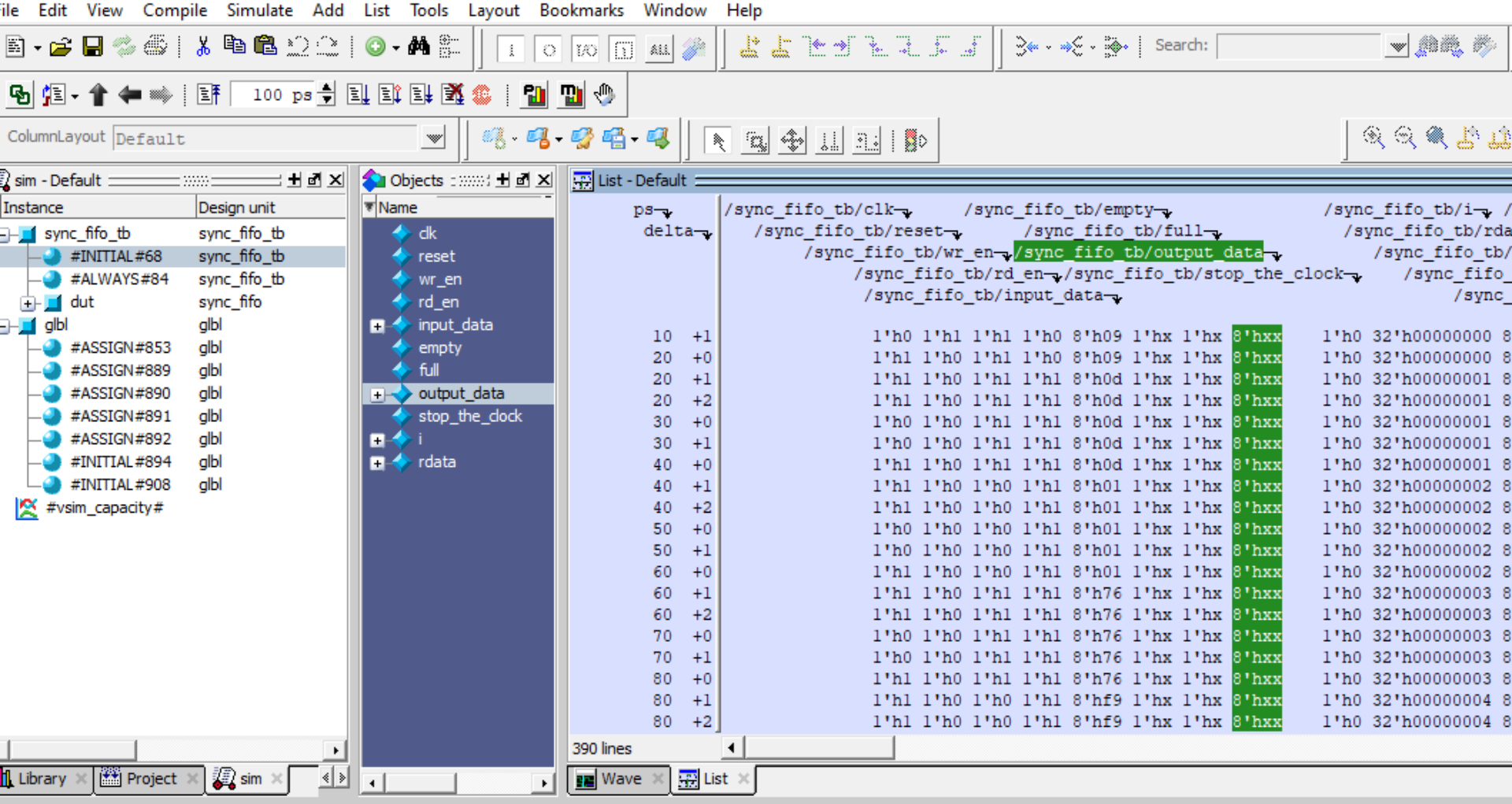
vsim -novopt work.sync_fifo_tb -sdfmax /dut=postSynth.sdf -sdfnoerror -L simprims_ver glbl

- Note:

  /UUT=netlist.sdf -> Apply delays only to design (UUT) within the testbech.

  -sdfmax -> Can also be used with -sdfmin or -sdftyp if needed.


le Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
Search:
100 ps
ColumnLayout AllColumns
sim - Default
Instance
Design unit
sync_fifo_tb sync_fifo_tb
#INITIAL#68 sync_fifo_tb
#ALWAYS#84 sync_fifo_tb
dut sync_fifo
glbl glbl
#ASSIGN#853 glbl
#ASSIGN#889 glbl
#ASSIGN#890 glbl
#ASSIGN#891 glbl
#ASSIGN#892 glbl
#INITIAL#894 glbl
#INITIAL#908 glbl
#vsim_capacity#
Objects
Name
clk
reset
wr_en
rd_en
input_data
empty
full
output_data
stop_the_clock
i
rdata
List - Default
ps
delta
/sync_fifo_tb/clk
/sync_fifo_tb/empty
/sync_fifo_tb/reset
/sync_fifo_tb/full
/sync_fifo_tb/wr_en
/sync_fifo_tb/output_data
/sync_fifo_tb/rd_en
/sync_fifo_tb/stop_the_cl
/sync_fifo_tb/input_data
0 +0 l'hx l'hx l'hx l'hx 8'hxx l'hx l'hx 8'hxx
0 +1 l'hx l'hx l'hx l'hx 8'hxx l'hx l'hx 8'hxx
0 +2 l'h1 l'h1 l'h0 l'h0 8'hxx l'hx l'hx 8'hxx
0 +3 l'h1 l'h1 l'h1 l'h0 8'h09 l'hx l'hx 8'hxx
0 +4 l'h1 l'h1 l'h1 l'h0 8'h09 l'hx l'hx 8'hxx
10 +0 l'h0 l'h1 l'h1 l'h0 8'h09 l'hx l'hx 8'hxx
10 +1 l'h0 l'h1 l'h1 l'h0 8'h09 l'hx l'hx 8'hxx
20 +0 l'h1 l'h0 l'h1 l'h0 8'h09 l'hx l'hx 8'hxx
20 +1 l'h1 l'h0 l'h1 l'h1 8'h0d l'hx l'hx 8'hxx
20 +2 l'h1 l'h0 l'h1 l'h1 8'h0d l'hx l'hx 8'hxx
30 +0 l'h0 l'h0 l'h1 l'h1 8'h0d l'hx l'hx 8'hxx
30 +1 l'h0 l'h0 l'h1 l'h1 8'h0d l'hx l'hx 8'hxx
40 +0 l'h1 l'h0 l'h1 l'h1 8'h0d l'hx l'hx 8'hxx
40 +1 l'h1 l'h0 l'h0 l'h1 8'h01 l'hx l'hx 8'hxx
40 +2 l'h1 l'h0 l'h0 l'h1 8'h01 l'hx l'hx 8'hxx
50 +0 l'h0 l'h0 l'h0 l'h1 8'h01 l'hx l'hx 8'hxx
50 +1 l'h0 l'h0 l'h0 l'h1 8'h01 l'hx l'hx 8'hxx
60 +0 l'h1 l'h0 l'h0 l'h1 8'h01 l'hx l'hx 8'hxx
60 +1 l'h1 l'h0 l'h1 l'h1 8'h76 l'hx l'hx 8'hxx
390 lines
Library
Project
sim
Wave
List
Transcript
[840] clk i = 41 rd_en=1 rdata=0xx
[840] clk i = 42 wr_en = 1 data_in=0xb5
[860] clk i = 43 wr_en = 0 data_in=0xd0
[860] clk i = 43 rd_en=1 rdata=0xx
[880] clk i = 43 rd_en=0 rdata=0xx
[880] clk i = 44 wr_en = 0 data_in=0xab
[900] clk i = 45 wr_en = 0 data_in=0xfd


File Edit View Compile Simulate Add List Tools Layout Bookmarks Window Help
Search:
100 ps
ColumnLayout Default
sim - Default
Instance
Design unit
sync_fifo_tb sync_fifo_tb
#INITIAL#68 sync_fifo_tb
#ALWAYS#84 sync_fifo_tb
dut sync_fifo
glbl glbl
#ASSIGN#853 glbl
#ASSIGN#889 glbl
#ASSIGN#890 glbl
#ASSIGN#891 glbl
#ASSIGN#892 glbl
#INITIAL#894 glbl
#INITIAL#908 glbl
#vsim_capacity#
Objects
Name
clk
reset
wr_en
rd_en
input_data
empty
full
output_data
stop_the_clock
i
rdata
List - Default
ps
delta
/sync_fifo_tb/clk
/sync_fifo_tb/reset
/sync_fifo_tb/wr_en
/sync_fifo_tb/rd_en
/sync_fifo_tb/input_data
/sync_fifo_tb/empty
/sync_fifo_tb/full
/sync_fifo_tb/output_data
/sync_fifo_tb/stop_the_clock
/sync_fifo_tb/i
10 +1 1'h0 1'hl 1'hl 1'h0 8'h09 1'hx 1'hx 8'hxx 1'h0 32'h00000000
20 +0 1'hl 1'h0 1'hl 1'h0 8'h09 1'hx 1'hx 8'hxx 1'h0 32'h00000000
20 +1 1'hl 1'h0 1'hl 1'hl 8'h0d 1'hx 1'hx 8'hxx 1'h0 32'h00000001
20 +2 1'hl 1'h0 1'hl 1'hl 8'h0d 1'hx 1'hx 8'hxx 1'h0 32'h00000001
30 +0 1'h0 1'h0 1'hl 1'hl 8'h0d 1'hx 1'hx 8'hxx 1'h0 32'h00000001
30 +1 1'h0 1'h0 1'hl 1'hl 8'h0d 1'hx 1'hx 8'hxx 1'h0 32'h00000001
40 +0 1'hl 1'h0 1'hl 1'hl 8'h0d 1'hx 1'hx 8'hxx 1'h0 32'h00000001
40 +1 1'hl 1'h0 1'h0 1'hl 8'h01 1'hx 1'hx 8'hxx 1'h0 32'h00000002
40 +2 1'hl 1'h0 1'h0 1'hl 8'h01 1'hx 1'hx 8'hxx 1'h0 32'h00000002
50 +0 1'h0 1'h0 1'h0 1'hl 8'h01 1'hx 1'hx 8'hxx 1'h0 32'h00000002
50 +1 1'h0 1'h0 1'h0 1'hl 8'h01 1'hx 1'hx 8'hxx 1'h0 32'h00000002
60 +0 1'hl 1'h0 1'h0 1'hl 8'h01 1'hx 1'hx 8'hxx 1'h0 32'h00000002
60 +1 1'hl 1'h0 1'hl 1'hl 8'h76 1'hx 1'hx 8'hxx 1'h0 32'h00000003
60 +2 1'hl 1'h0 1'hl 1'hl 8'h76 1'hx 1'hx 8'hxx 1'h0 32'h00000003
70 +0 1'h0 1'h0 1'hl 1'hl 8'h76 1'hx 1'hx 8'hxx 1'h0 32'h00000003
70 +1 1'h0 1'h0 1'hl 1'hl 8'h76 1'hx 1'hx 8'hxx 1'h0 32'h00000003
80 +0 1'hl 1'h0 1'hl 1'hl 8'h76 1'hx 1'hx 8'hxx 1'h0 32'h00000003
80 +1 1'hl 1'h0 1'h0 1'hl 8'hf9 1'hx 1'hx 8'hxx 1'h0 32'h00000004
80 +2 1'hl 1'h0 1'h0 1'hl 8'hf9 1'hx 1'hx 8'hxx 1'h0 32'h00000004
390 lines
Library
Project
sim
Wave
List
Transcript
[840] clk i = 42 wr_en = 1 data_in=0xb5
[860] clk i = 43 wr_en = 0 data_in=0xd0
[860] clk i = 43 rd_en=1 rdata=0xx
[880] clk i = 43 rd_en=0 rdata=0xx
[880] clk i = 44 wr_en = 0 data_in=0xab

Vivado Design Suite User Guide

Design Analysis and Closure Techniques

UG906 (v2022.1) May 4, 2022

Figure 43: **Timing Paths Example**

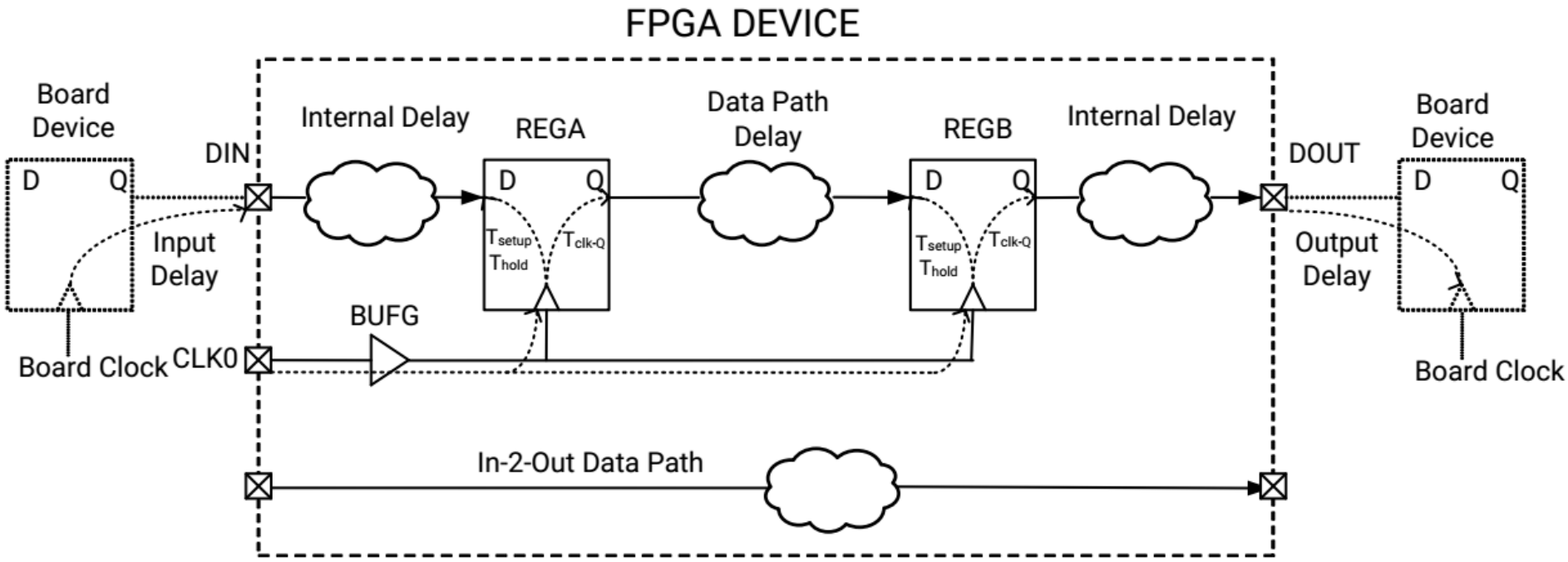
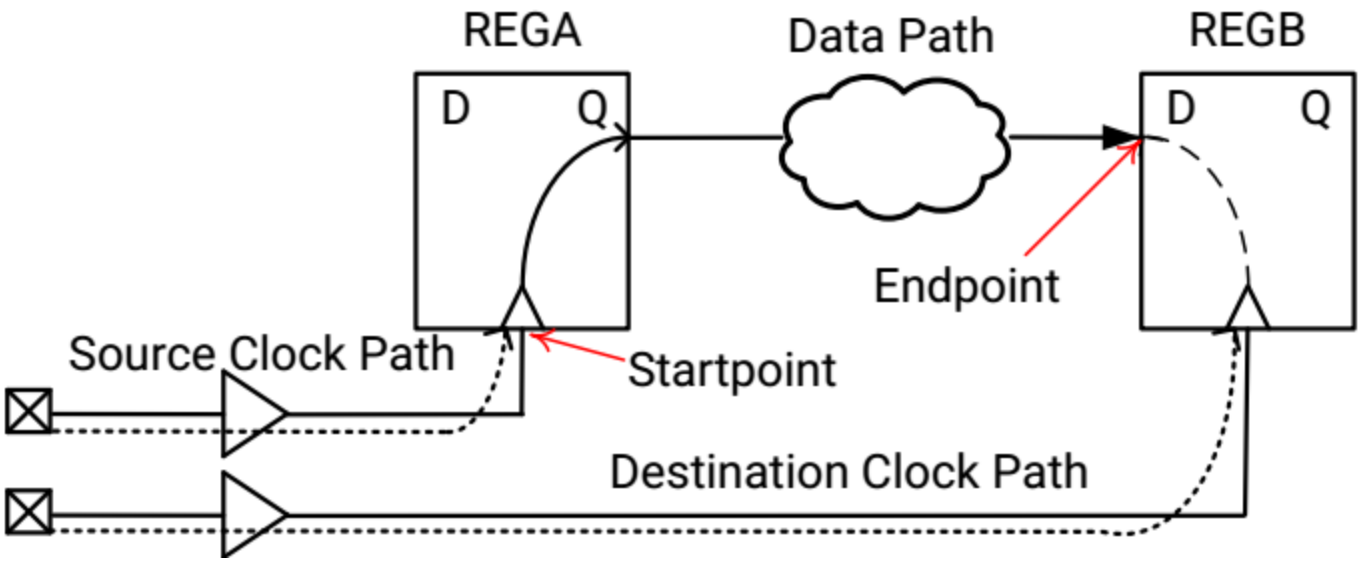


Figure 44: **Typical Timing Path**



Typical Slack Equaton

- A **positve** setup slack occurs when the data arrives before the required tme.
- Hold slack is positve when the new data arrives after the required time.

Data Required Time (setup)	**=**	**capture edge time** **+ destination clock path delay** **- clock uncertainty** **- setup time**
Data Arrival Time (setup)	=	launch edge time + source clock path delay + datapath delay
Slack (setup)	=	Data Required Time - Data Arrival Time

Clock Uncertainty

Clock uncertainty is the total amount of possible time variation between any pair of clock edges. The uncertainty consists of the computed clock jitter (system, input, and discrete); the phase error introduced by certain hardware primitives; and any clock uncertainty specified by the user in the design constraints (`set_clock_uncertainty`).

Phase Shift in Timing Reports

A positive phase shift moves the source clock edge forward, delaying the clock edge. A negative phase shift moves the source clock edge backward. The modification of the clock waveform result in potentially different clock edges being used by the static timing analysis for the source and capture clocks.

- No phase shift

```
vivado% set_property CLKOUT0_PHASE 0.000 [get_cells qpll/plle2_adv_inst]
vivado% report_timing
...
(clock clkout0 rise edge) 0.000 0.000 r
...
        MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)
                                -5.411   5.903 r mmcm_inst/mmcm_adv_inst/
CLKOUT0
...
```

The source clock edge is 0.0 ns.

- Positive phase shift of 12.0 with `PHASESHIFT_MODE=WAVEFORM`

```
vivado% set_property CLKOUT0_PHASE 12.000 [get_cells qpll/plle2_adv_inst]
vivado% report_timing
...
(clock clkout0 rise edge) 0.333 0.333 r
...
    MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)
                            -5.411   5.903 r mmcm_inst/mmcm_adv_inst/CLKOUT0
...
```

The source clock edge is delayed by 0.333 ns (10 ns / 360 * 12.0).

Missing Logically / Physically Excluded Clock Groups Constraint

Multiple clocks are user generated or auto-derived on the source pin(s) <pin_names> but are not logically or physically exclusive with respect to one another. To have the static timing analysis match the behavior in hardware, there cannot be multiple clocks generated on the same pin(s). In such cases, the clocks should be defined as physically or logically exclusive. The list of clocks generated on the source pin(s) is: <clock_names>.

Description

When the output pin of a clocking primitive has multiple generated or auto-derived clocks present, these clocks cannot be available on hardware simultaneously. To match static timing analysis with hardware behavior, provide physically or logically exclusive clock group constraints between these clocks. Otherwise, some clock pairs will be timed although they do not exist in hardware.

Reading a Timing Path Report

Timing Path Summary Header Examples

The following figure shows an example of the Timing Path Summary Header in a text report.

Figure 48: **Timing Path Summary Header in Text Report**

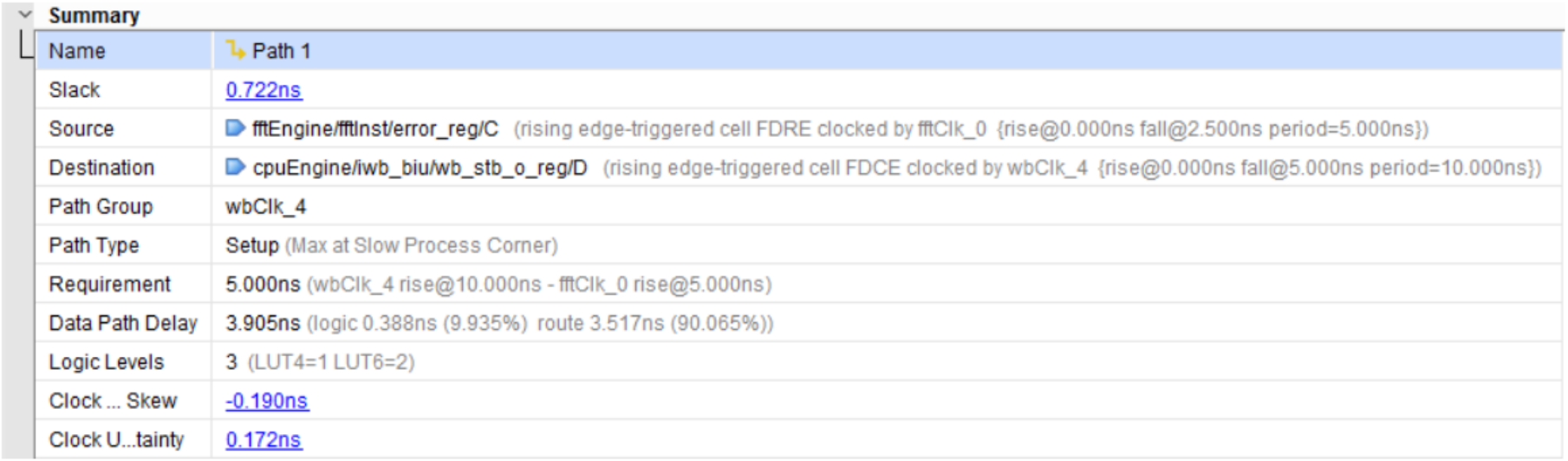
```
Slack (MET) :             0.722ns  (required time - arrival time)
  Source:                 fftEngine/fftInst/error_reg/C
                            (rising edge-triggered cell FDRE clocked by fftClk_0  {rise@0.000ns fall@2.500ns period=5.000ns})
  Destination:            cpuEngine/iwb_biu/wb_stb_o_reg/D
                            (rising edge-triggered cell FDCE clocked by wbClk_4  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             wbClk_4
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            5.000ns  (wbClk_4 rise@10.000ns - fftClk_0 rise@5.000ns)
  Data Path Delay:        3.905ns  (logic 0.388ns (9.935%)  route 3.517ns (90.065%))
  Logic Levels:           3  (LUT4=1 LUT6=2)
  Clock Path Skew:        -0.190ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    -1.471ns = ( 8.529 - 10.000 )
    Source Clock Delay      (SCD):    -2.117ns = ( 2.883 - 5.000 )
    Clock Pessimism Removal (CPR):    -0.836ns
  Clock Uncertainty:      0.172ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Discrete Jitter          (DJ):    0.077ns
    Phase Error              (PE):    0.120ns
```

The following figure shows an example of the Timing Path Summary header in the Vivado IDE.

Figure 49: **Timing Path Summary Header in Vivado IDE**

The following figure shows an example of the Timing Path Summary header in the Vivado IDE.

Figure 49: **Timing Path Summary Header in Vivado IDE**



Timing Path Summary Header Information

The Timing Path Summary header includes the following information:

- Slack

  A positive slack indicates that the path meets the path requirement, which is derived from th

Backup Slide

simprims_ver for Questa

simprims_ver for Questa (2): Results

compile_simlib.log - Notepad

File Edit Format View Help

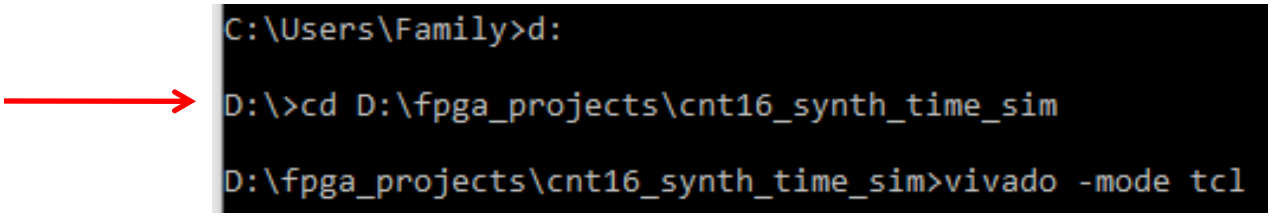
Library	Language	Mapped Library Name	Error(s)	Warning(s)
secureip	verilog	secureip	1	0
unisim	vhdl	unisim	3	0
unimacro	vhdl	unimacro	1	0
unifast	vhdl	unifast	1	0
unisim	verilog	unisims_ver	0	0
unimacro	verilog	unimacro_ver	0	0
unifast	verilog	unifast_ver	0	0
simprim	verilog	simprims_ver	0	0
xpm	vhdl	xpm	0	0

IMPORTANT: *The* `launch_simulation` *command launches integrated simulation for project-based designs. This command does not support Non-Project Mode. For more information, see Understanding Project and Non-Project Software Use Models.*

```
# //
# Loading project counter_16
# reading C:/questasim64_10.2c/win64/../modelsim.ini
# Loading project counter_16
# Compile of up_counter_16.v was successful.
QuestaSim> vsim -gui -novopt work.up_counter_16
# vsim -gui -novopt work.up_counter_16
# Refreshing D:/Questasim_projects/counter_16/work.up_counter_16
# Loading work.up_counter_16
add list -r /*
force -freeze sim:/up_counter_16/reset 1'h1 0
force -freeze sim:/up_counter_16/clock 1 0, 0 {25 ns} -r 50

VSIM 5>
```

```
1  vsim up_counter_16
2  add wave out
3  add wave clock
4  add wave reset
5  add list out
6  add list clock
7  add list reset
8  force -freeze clock 0 0, 1 {50 ns} -r 100
9  force reset 1
10 run 100
11 force reset 0
12 run 300
13 force reset 1
14 run 400
15 force reset 0
16 run 200
```




```
Vivado% read_verilog "cnt16.v"
read_verilog: Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 1088.910 ; gain = 0.000
D:/fpga_projects/cnt16_synth_time_sim/cnt16.v
Vivado% synth_design -top "cnt16" -part "xc7a35tcpg236-1"
```

```
Vivado% write_verilog -mode funcsim cnt16_netlist.v
D:/fpga_projects/cnt16_synth_time_sim/cnt16_netlist.v
Vivado% close_project
Vivado% exit
```

Thank You