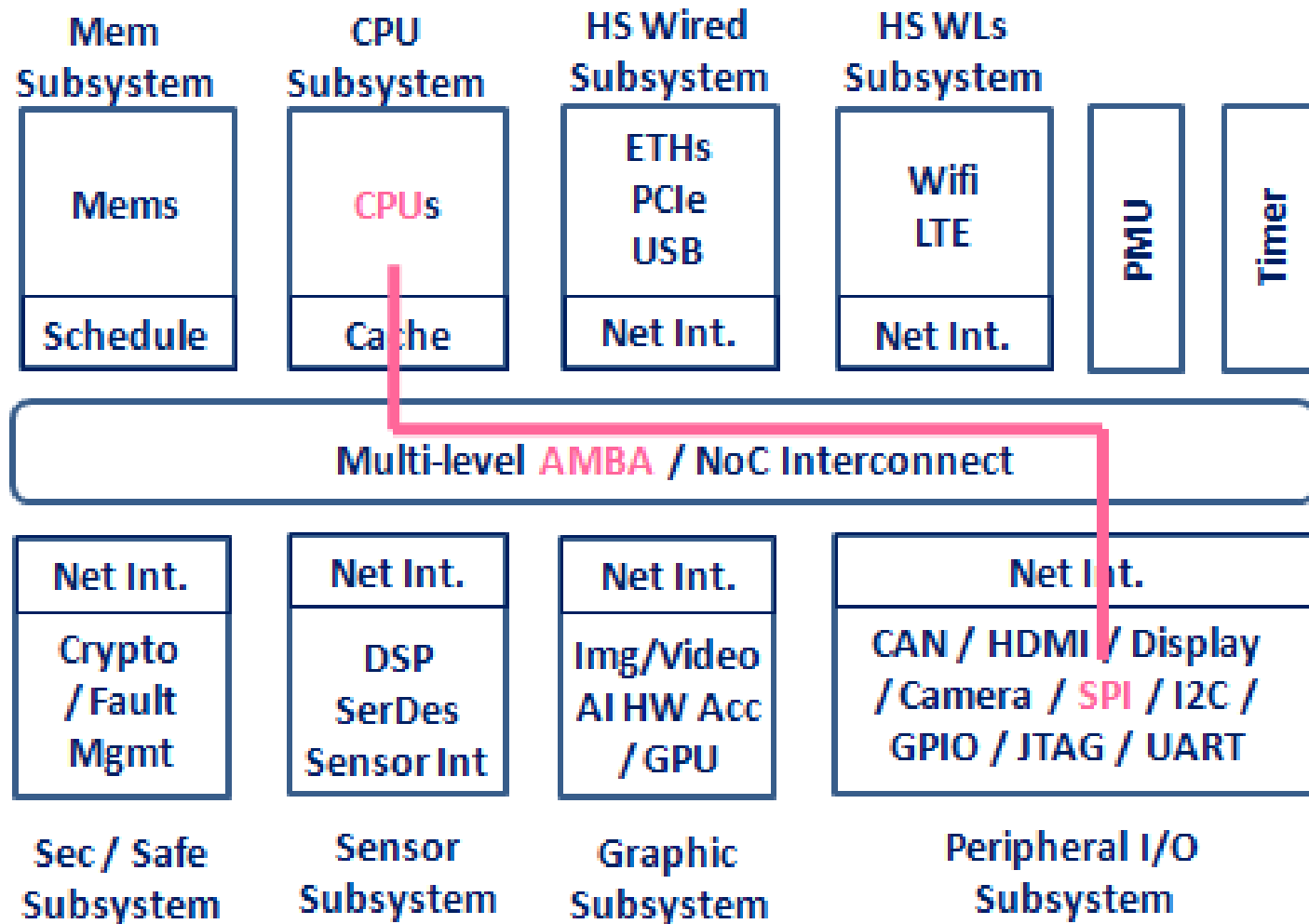


# **SPI Bus (Serial Peripheral Interface Bus)**

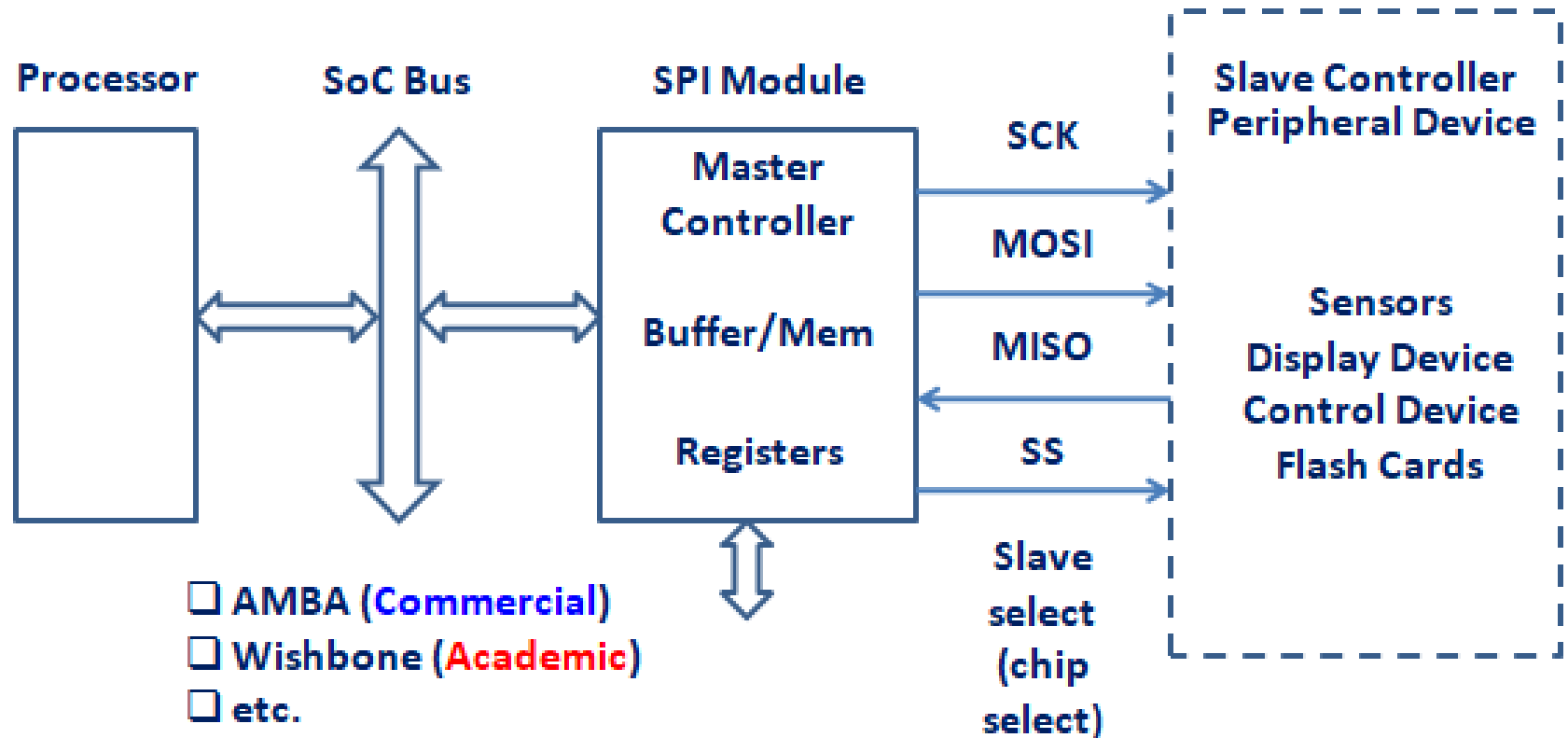
## **SoC - SPI**

Tuan Nguyen-viet

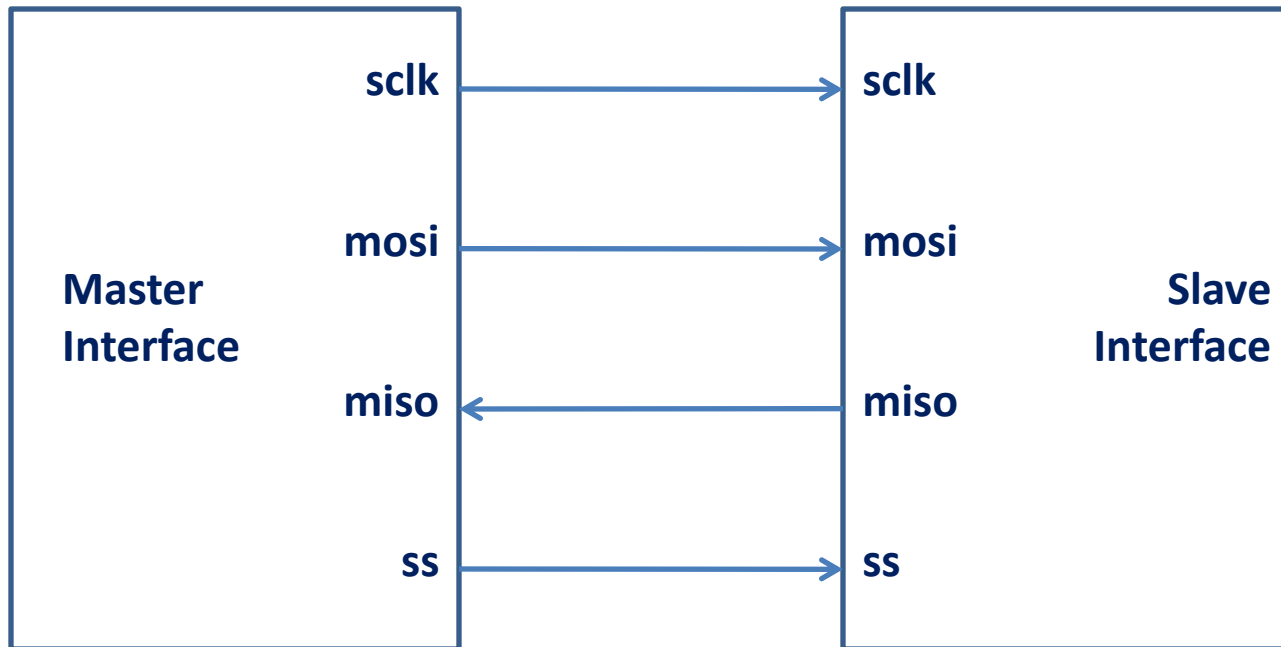
# Processor-SPI Interaction



# Processor-SPI Interaction

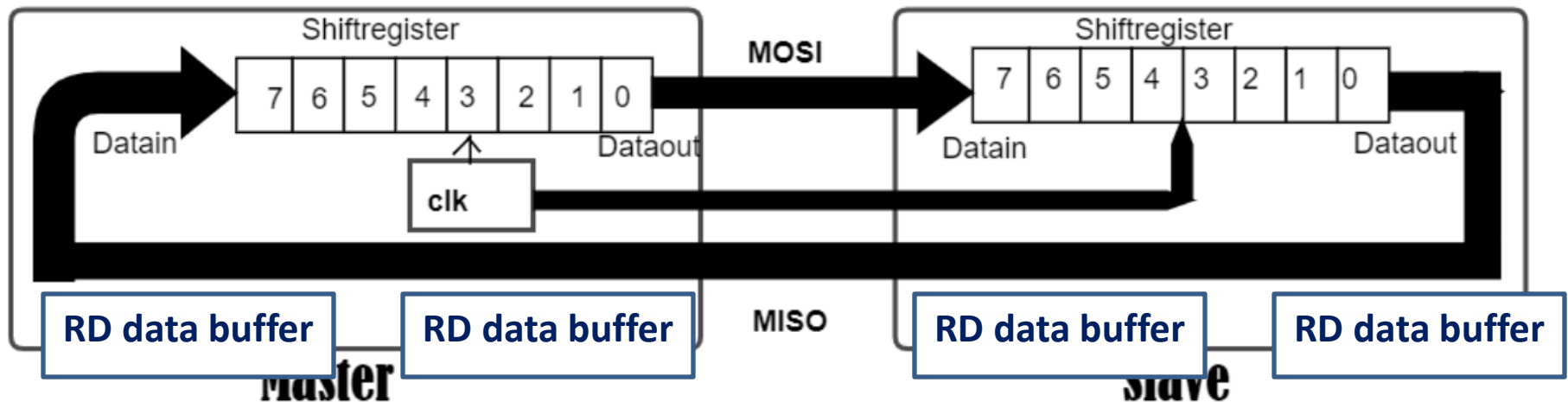


# SPI Master / Slave

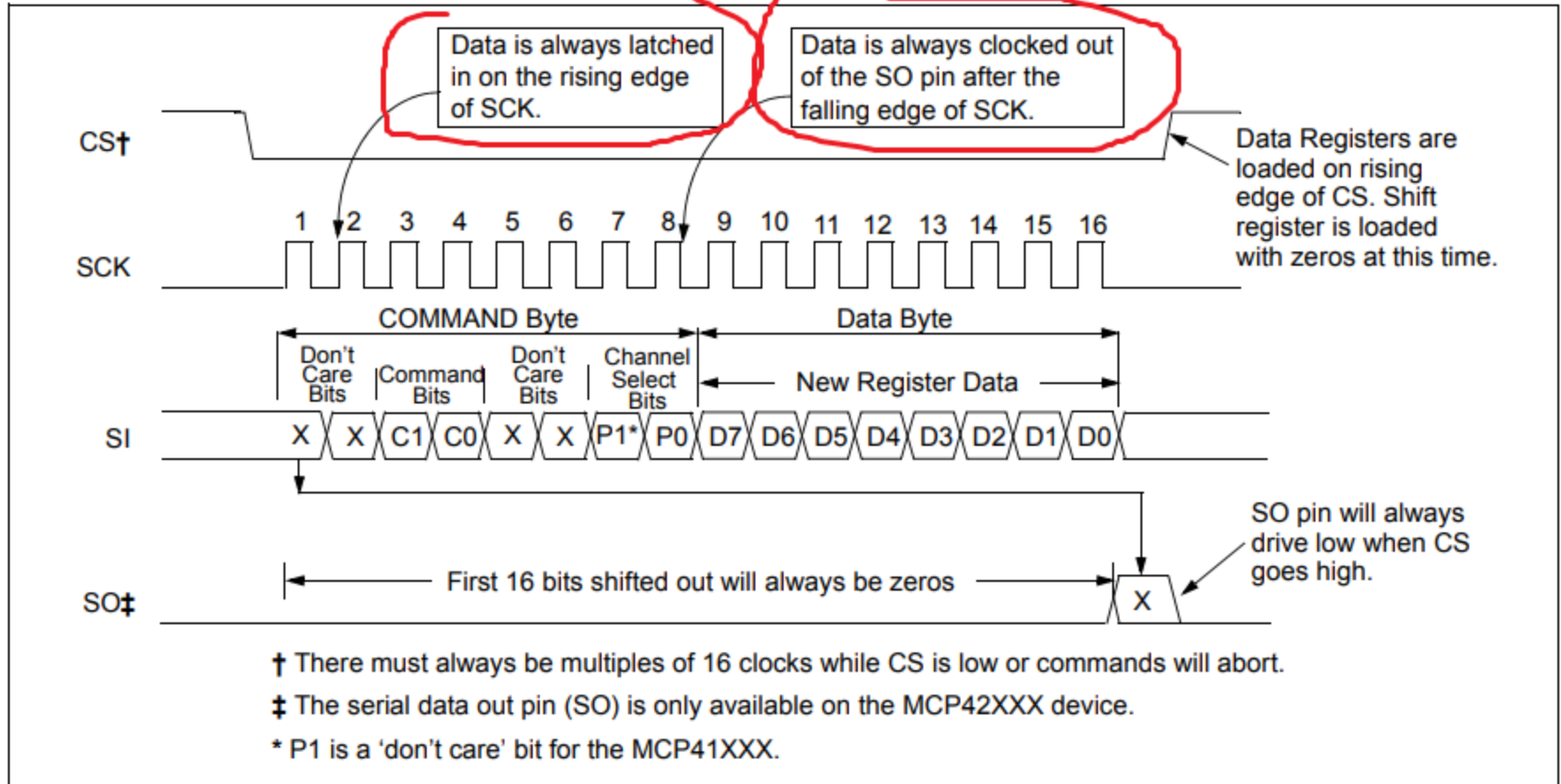


# 8-bit transfer in the SPI

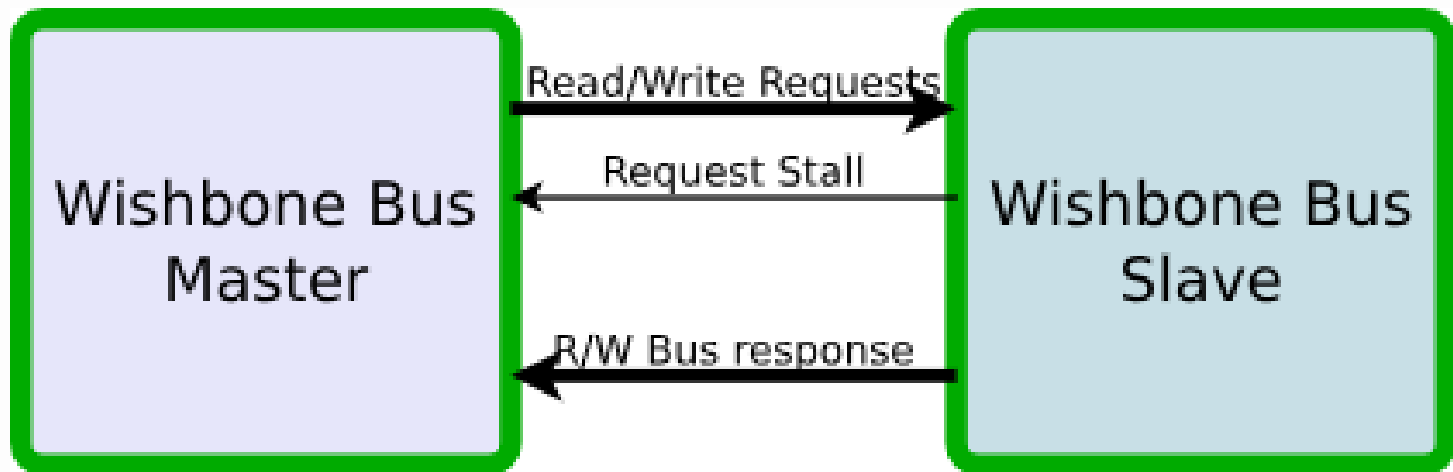
- **8-bit shift register** and **RD data buffer** is the key blocks of SPI interface.
- It is **single buffered** in the **transmit direction**
  - to ensure a new character is transferred
    - only after the transfer of the previous character is complete
  - and is **double-buffered** in the **receive direction**.



# A Typical Transfer Format



# Academic Wishbone

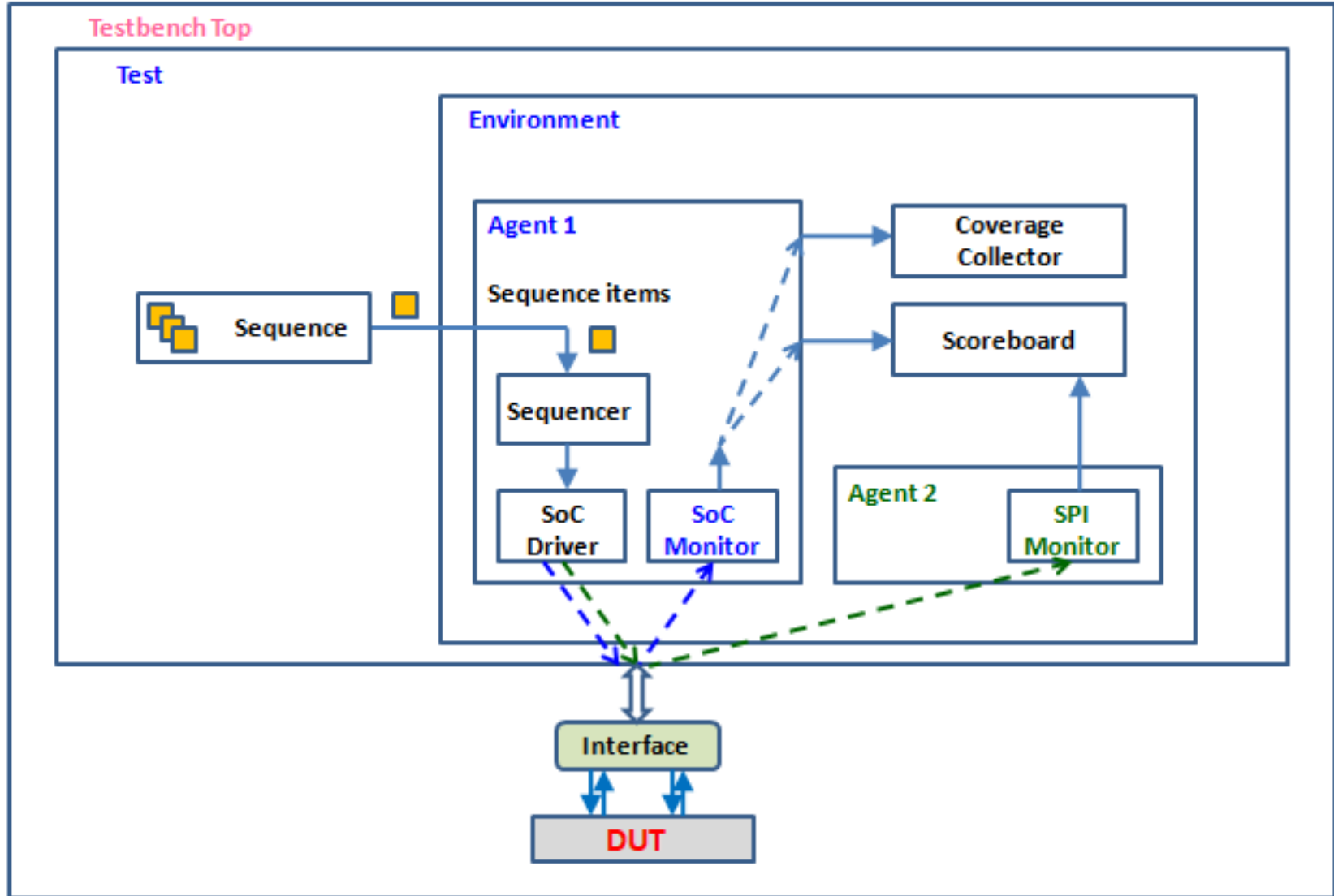


## Academic Wishbone (2)

Specification name	Our name	
CYC_O	o_wb_cyc	Signals from the master to the slave
STB_O	o_wb_stb	
WE_O	o_wb_we	
ADDR_O	o_wb_addr	
DATA_O	o_wb_data	
SEL_O	o_wb_sel	Signals returning to the master from the slave
STALL_I	i_wb_stall	
ACK_I	i_wb_ack	
DATA_I	i_wb_data	
ERR_I	i_wb_err	



# UVM Architecture



**Thank You**