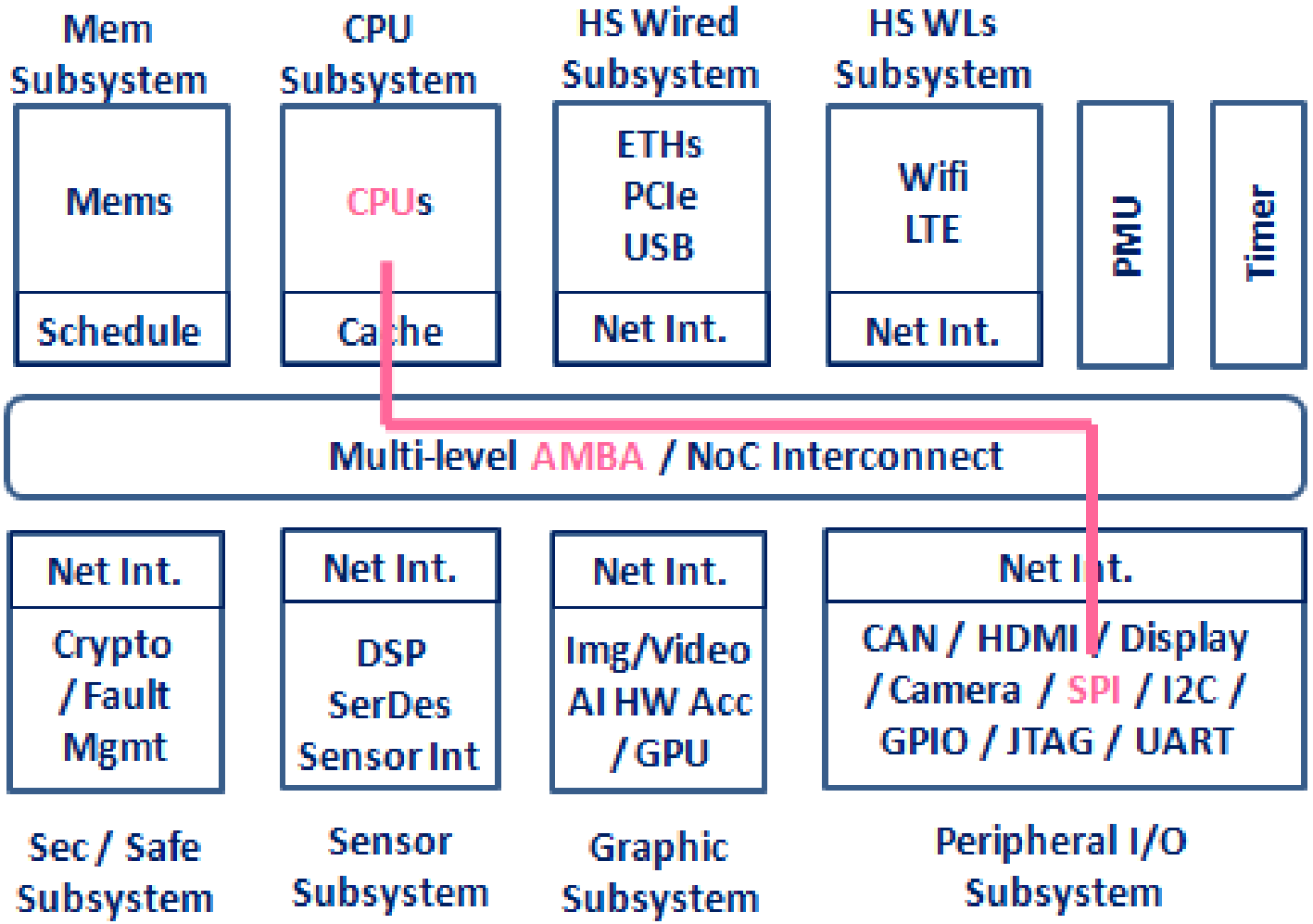
SPI Bus (Serial Peripheral Interface Bus)

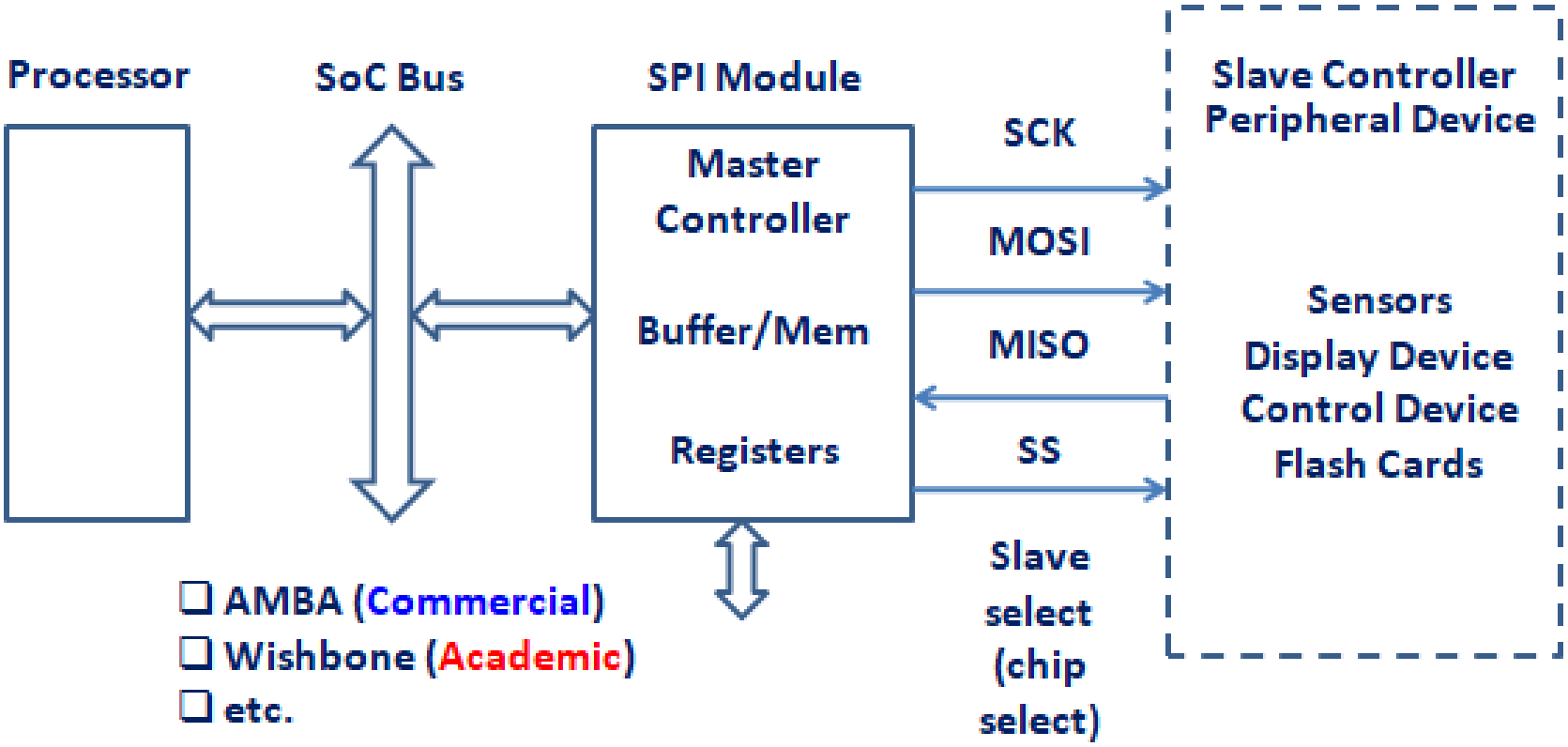
SoC - SPI

Tuan Nguyen-viet

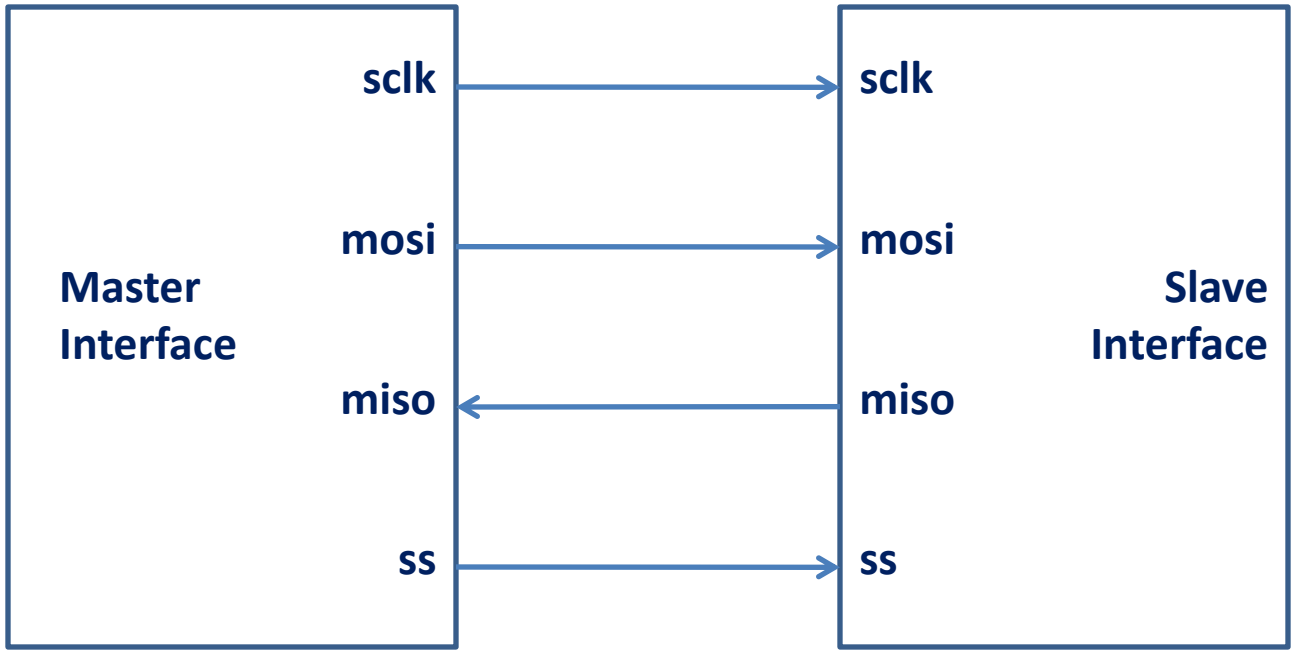
Processor-SPI Interaction



Processor-SPI Interaction

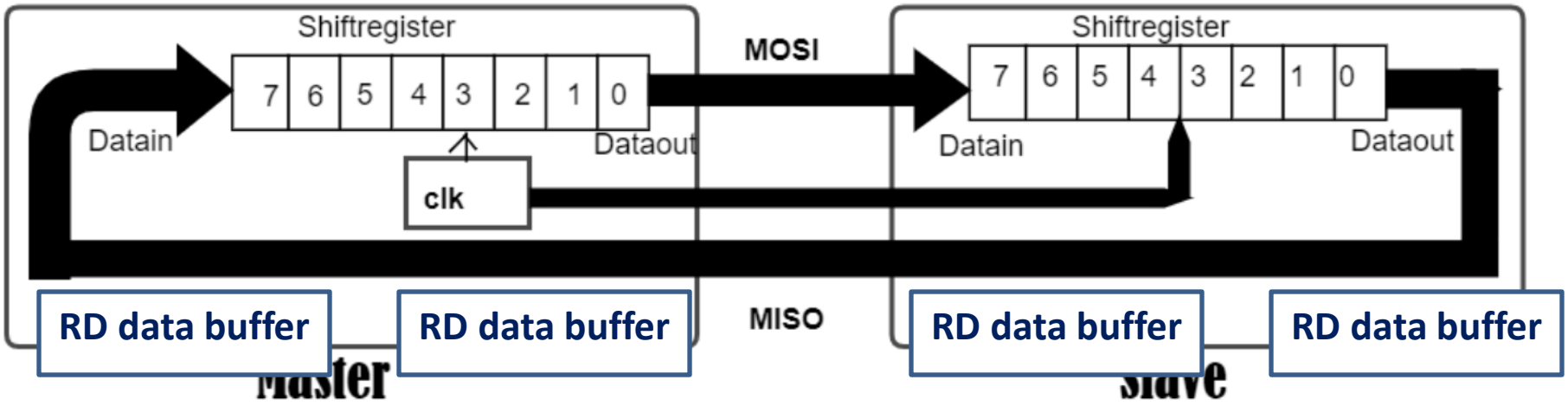


SPI Master / Slave

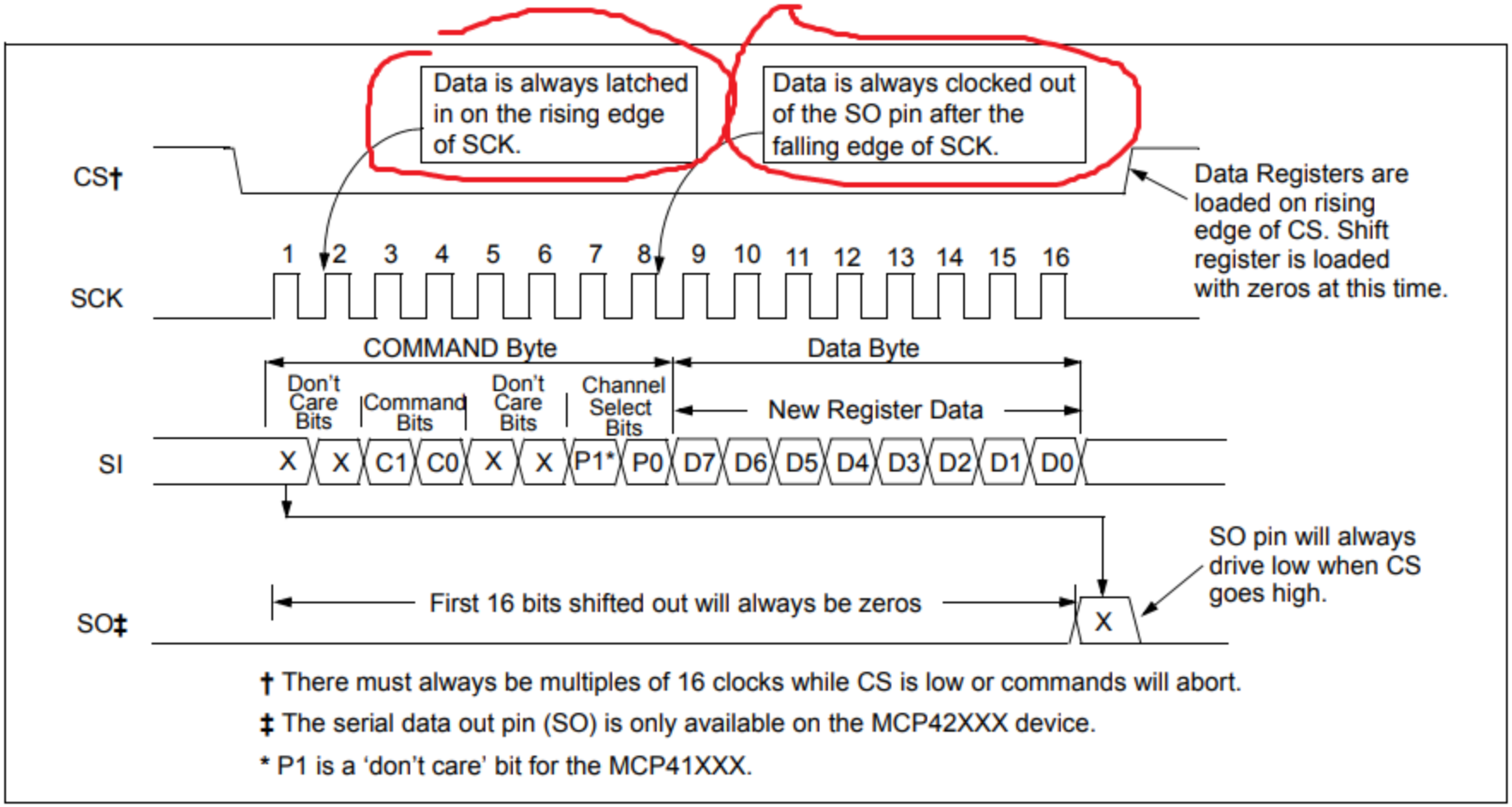


8-bit transfer in the SPI

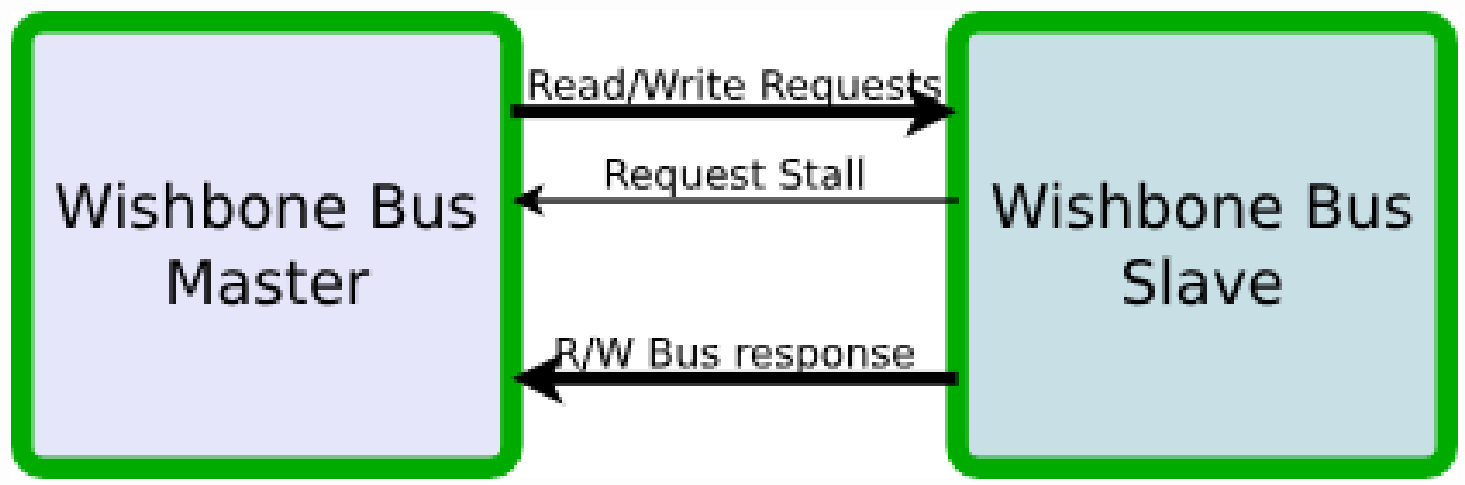
- **8-bit shift register** and **RD data buffer** is the key blocks of SPI interface.
- It is single buffered in the transmit direction
  - to ensure a new character is transferred
    - only after the transfer of the previous character is complete
  - and is double-buffered in the receive direction.



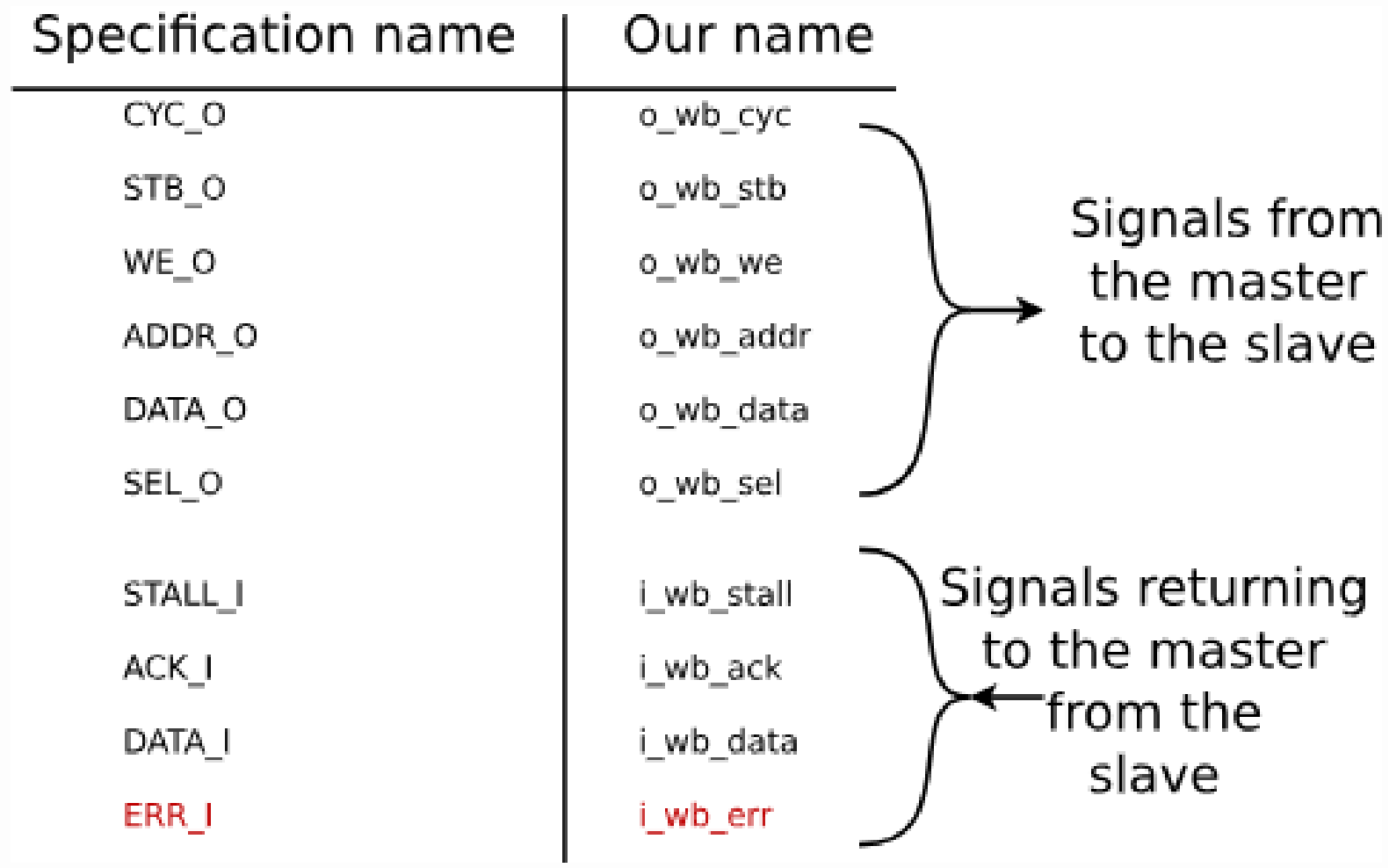
A Typical Transfer Format



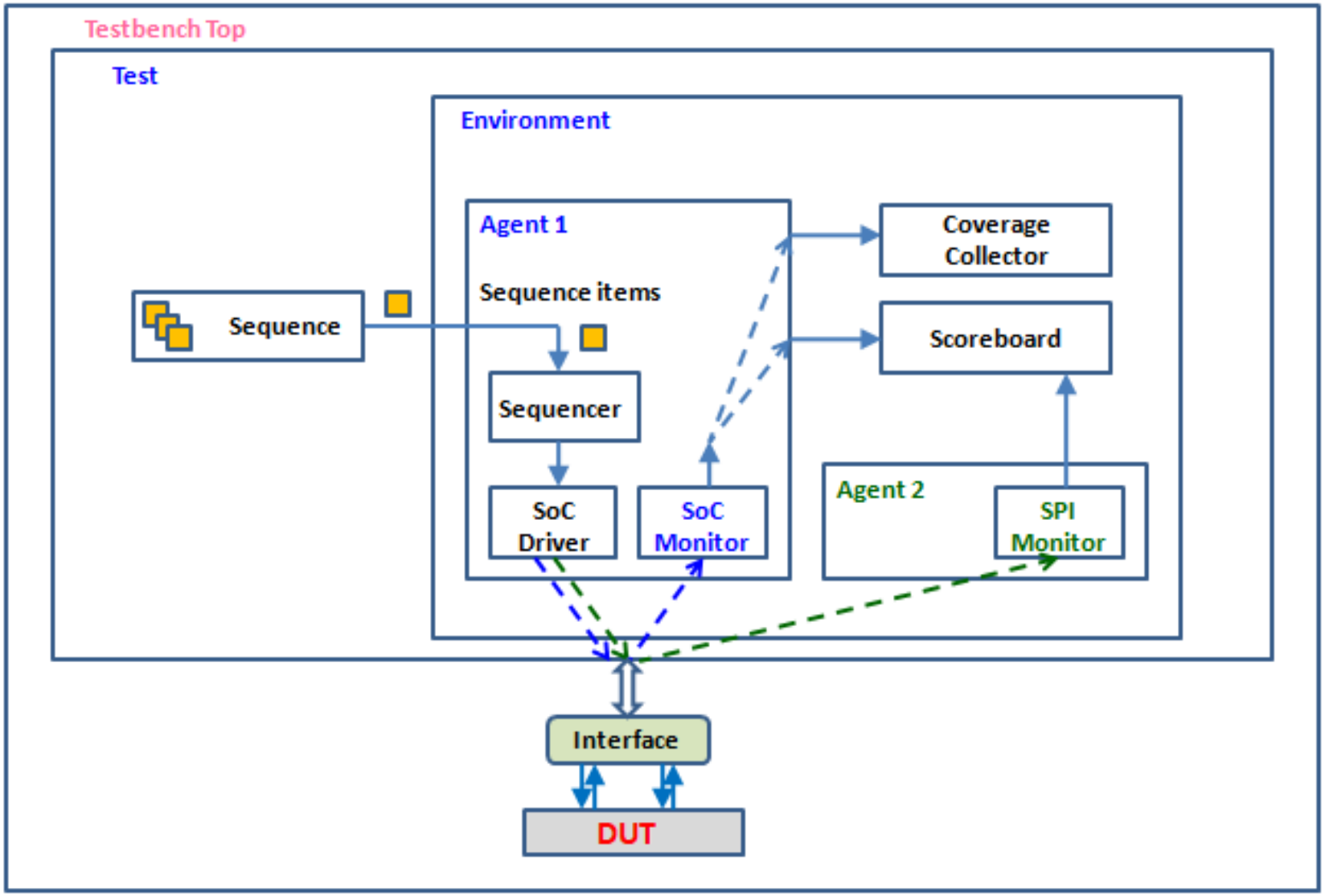
Academic Wishbone



Academic Wishbone (2)



UVM Architecture



Thank You