DPRAM (Dual Port RAM)
For SW Engineers

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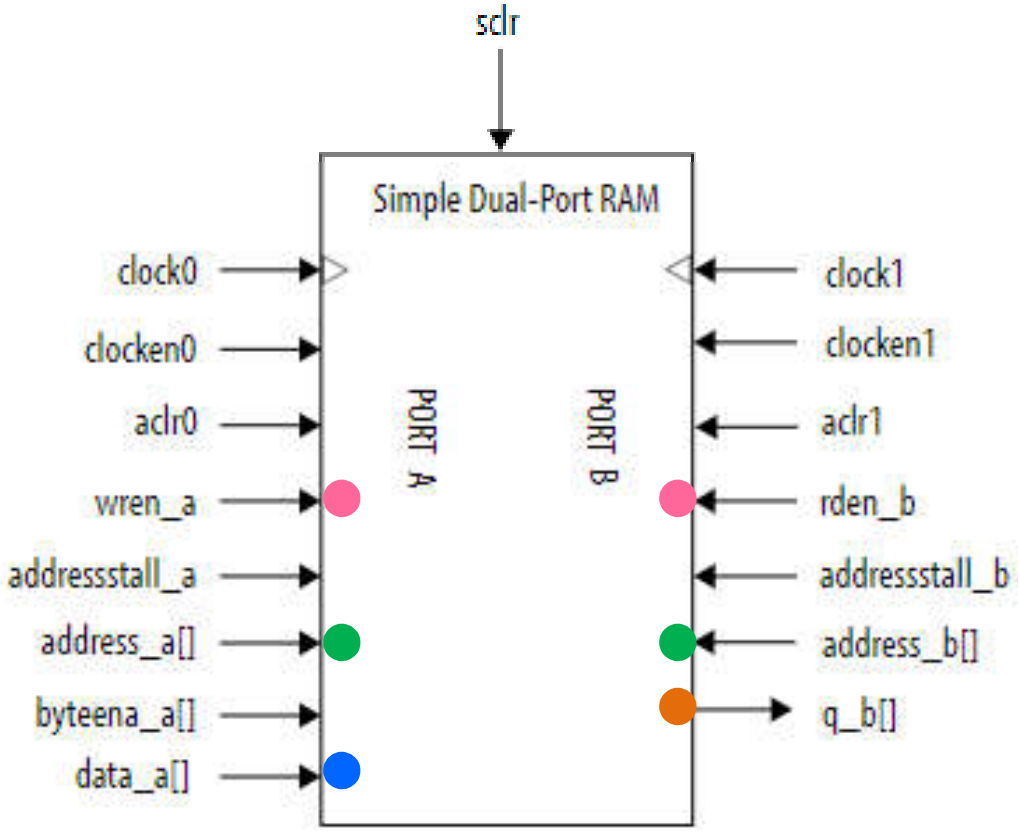
Simple DP RAM

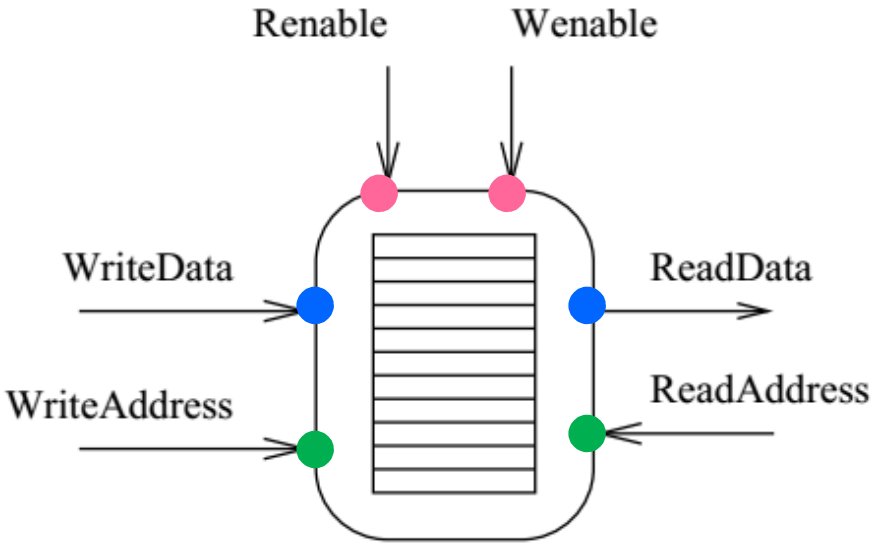
- In **Simple** DP RAM mode, Port in and **Port out** are available with
  - two **address ports** (one at Port in and one at **Port out**)
  - and one **data output port** (only at **Port out**).
- Port in is the write port that performs write operation according to the write address.
- **Port out** is the **read port** that
  - performs **read operation** according to the **read address** and
  - outputs the data.



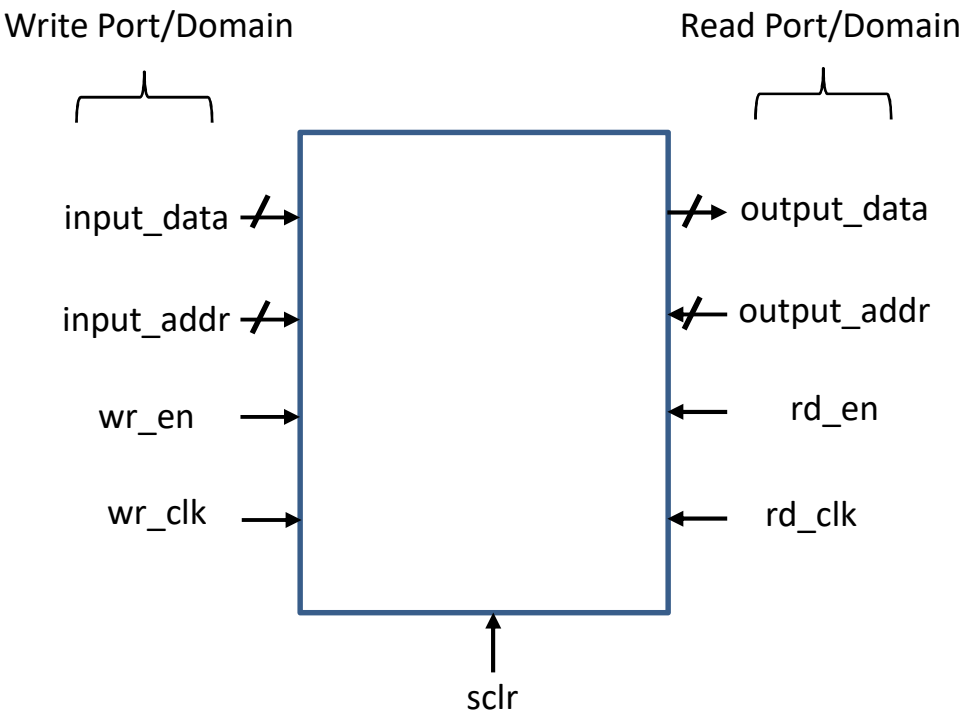
REF: https://www.intel.com/content/www/us/en/docs/programmable/772350/23-1/simple-dual-port-ram.html

Dual Port RAM

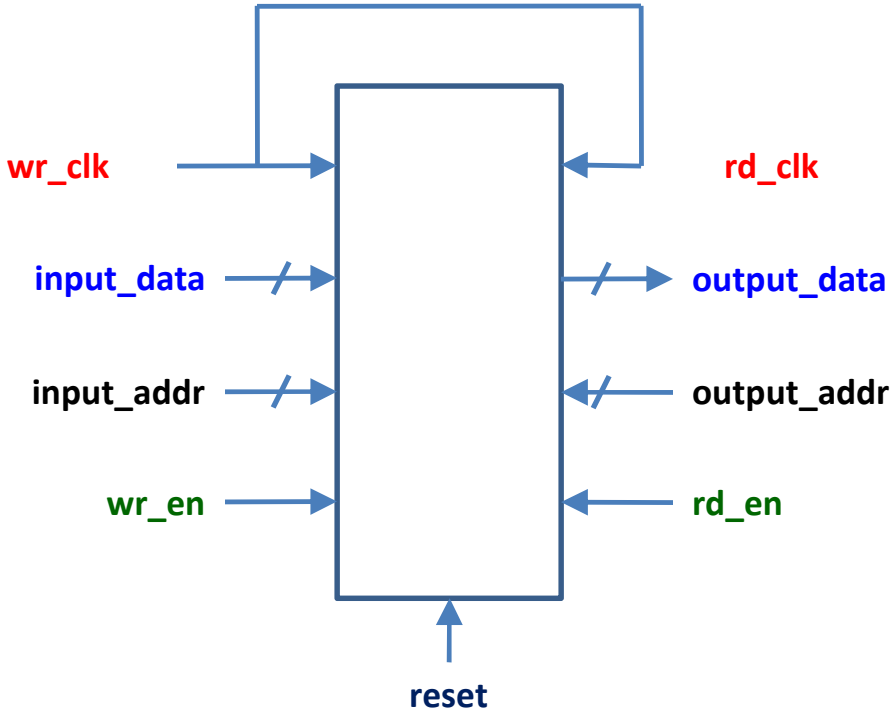
- DP RAM (Random Access Memory) is a type of memory
  - that has two independent access ports,
    - which allows two different **devices** or **circuits** to ***read from*** or ***write to*** the memory **at the same time**.
- In a DP RAM,
  - **each port** has its own set of *address* and *control* signals
    - and can access the memory independently of the **other port**.



Simple DP RAM (2)



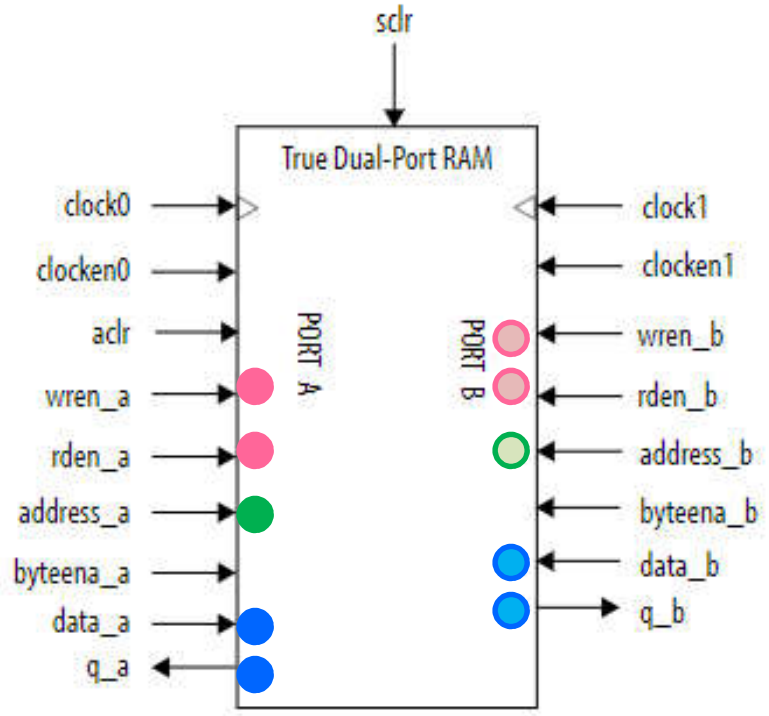
Simple DP RAM (3)



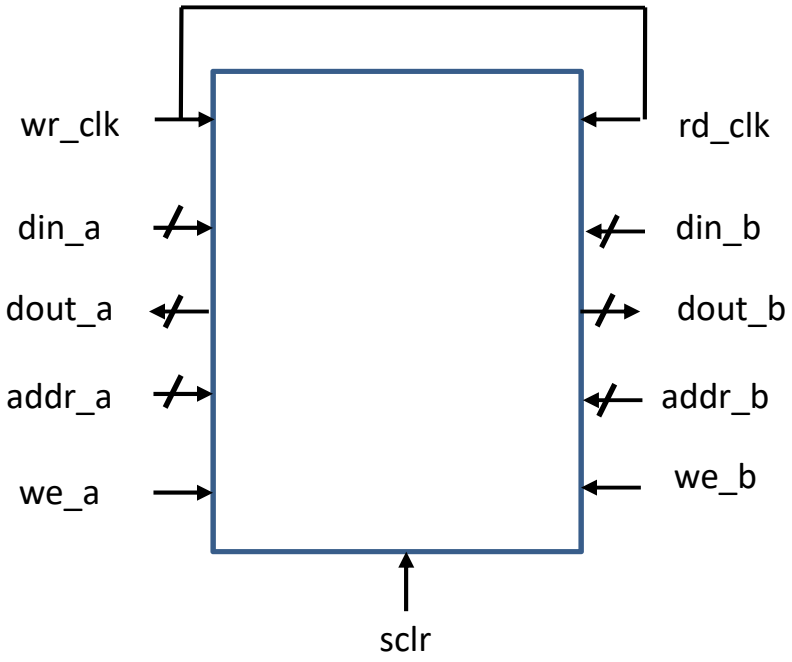
Task: Do a UVM Testbench for DPRAM shown above, using **.do** file to run the simulation.

True DPRAM

- In True DP RAM mode, Port A and Port B are available with
  - two address ports (one at Port A and one at Port B)
  - and two data output ports (one at Port A and one at Port B).
- Both Port A and Port B can perform read and write operations
  - according to the address provided from its address port.
- ***The same address*** is always referenced
  - when read and write operations are happening
    - at ***the same time***
      - at the same port.



True DPRAM (2)



Sample: We will do a UVM Testbench for TDPRAM shown above.

Typical Applications

It can be used in a variety of applications,

- such as in **communication systems**,
  - where data needs to be transferred
    - between multiple **devices** or **circuits** simultaneously.

- It can also be used in **digital signal processing** (**DSP**) applications,
  - where data needs to be processed by multiple **circuits** in parallel.

Types of DPRAM

- DP RAM can be implemented
  - as a Single Block DP RAM
  - or as a Dual Block DP RAM.
- In a Single Block DP RAM,
    - the memory array is shared between both ports,
  - whereas in a Dual Block DP RAM,
    - there are two separate memory arrays, one for each port.

- DP RAM can also be synchronous or asynchronous.
  - **Synchronous** DP RAMs have a **clock signal** that synchronizes access to both ports,
  - while asynchronous DP RAMs do not use a clock signal
    - and instead rely on control signals to coordinate access to both ports.

Types of DPRAM (2)

- In general, DP RAMs provide a flexible and efficient way to share data between multiple devices or circuits.

- DP RAM can be used to implement other types of memory as well, such as
  - **FIFOs** (First-In, First-Out)
  - and LIFO (Last-In, First-Out)
    - by controlling the read and write pointers for each port.

Dual-ported RAM

(https://en.wikipedia.org/wiki/Dual-ported_RAM)

- Dual-ported RAM (DPRAM), also called dual-port RAM,
  - is a type of random-access memory (RAM)
    - that can be accessed via two different buses.
- A **simple** DPRAM may allow only *read access* through one of the ports and *write access* through the other,
  - in which case *the same* memory location cannot be accessed simultaneously through the ports
    - since a *write operation*
      - modifies the data
      - and therefore needs to be synchronized with
        - » a *read*
        - » or another *write operation*.

Dual-ported RAM (2)

(https://en.wikipedia.org/wiki/Dual-ported_RAM)

- A dual-port RAM may be built from single-port memory cells
  - to reduce cost or circuit complexity, and the performance penalty associated with it,
    - which may still allow *simultaneous* read and write accesses to *different* memory locations
      - depending on the partitioning of the **memory array**
      - and having duplicate decoder paths to the partitions.

Dual-ported RAM (3)

(https://en.wikipedia.org/wiki/Dual-ported_RAM)

- A **true** dual-port memory has **two *independent*** ports,
  - which means that the **memory array** is built from dual-port memory-cells,
    - and the *address*, *data*, and *control* lines of the two ports
      - are connected to ***dedicated*** IO controllers
  - so that *the same* memory location can be read through the ports simultaneously.
- A write operation through one of the ports
  - still needs to be synchronized with
    - a read or write operation
      - to *the same* memory location
        - » through the other port.

Examples of DPRAM

DPRAMs have many real-life applications, some of which include:

1. DSP systems:
   - Regs: DSP systems often require fast and efficient memory access
     - to perform operations on large amounts of data.
   - DPRAMs can be used in these systems to allow multiple DSP circuits **to access the memory** *simultaneously*,
     - improving performance
     - and reducing latency.

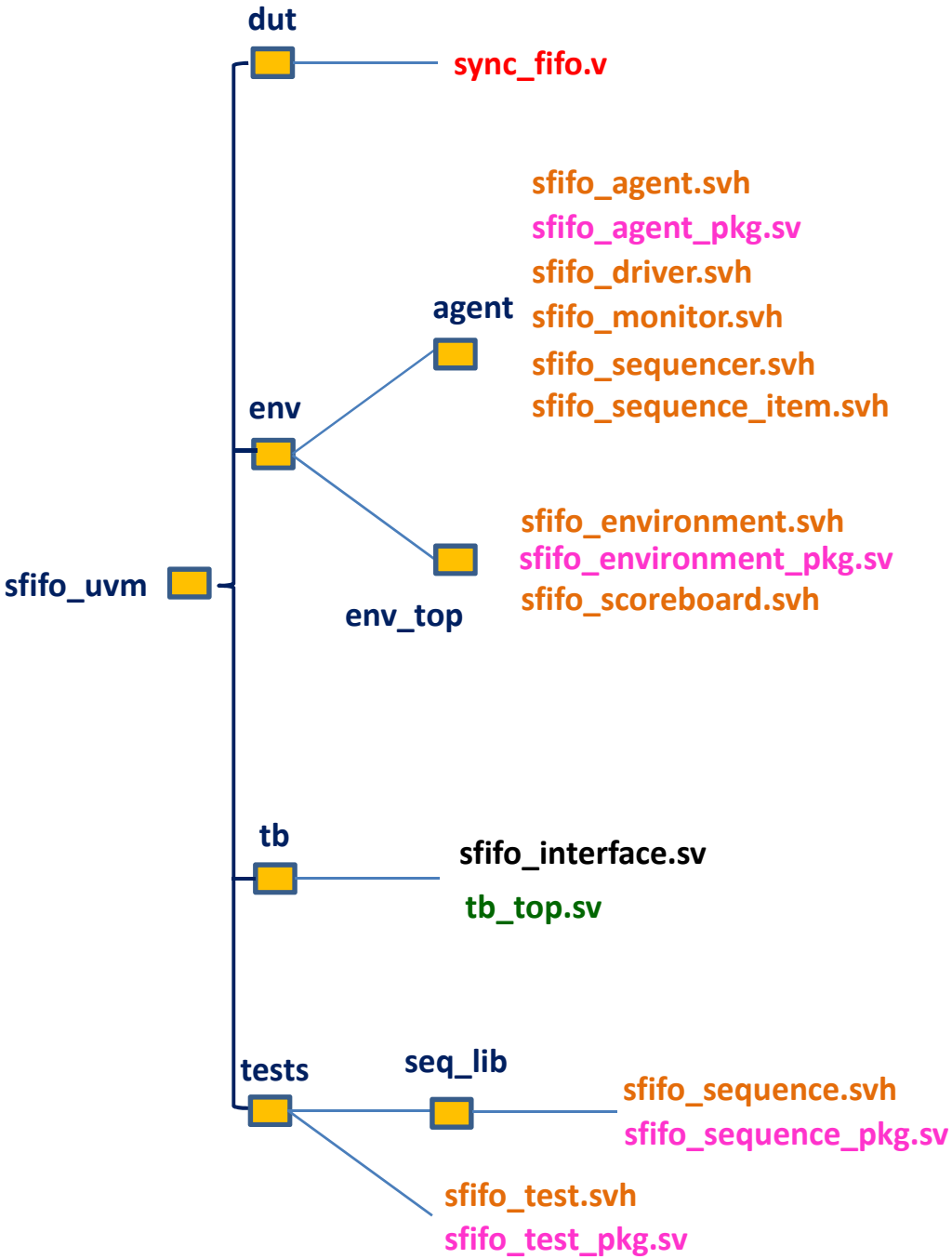
2. Network switches and routers:
   - DPRAM can be used to store and manage
     - *routing tables* and other network-related data
       - in switches and routers.
   - With multiple ports, the RAM can be accessed by both the ***control plane*** and the ***data plane***, improving overall system performance and throughput.

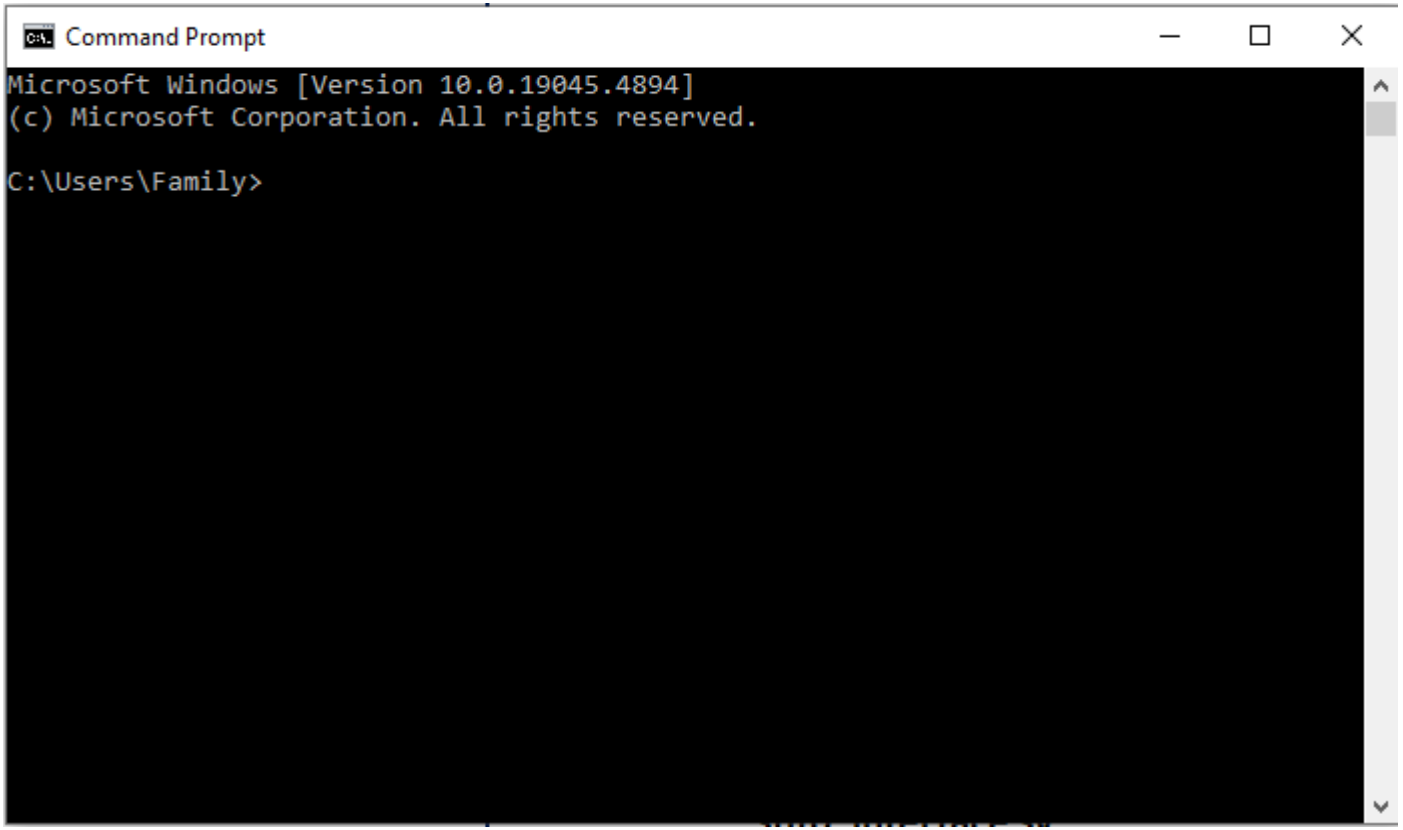
Examples of DPRAM (2)

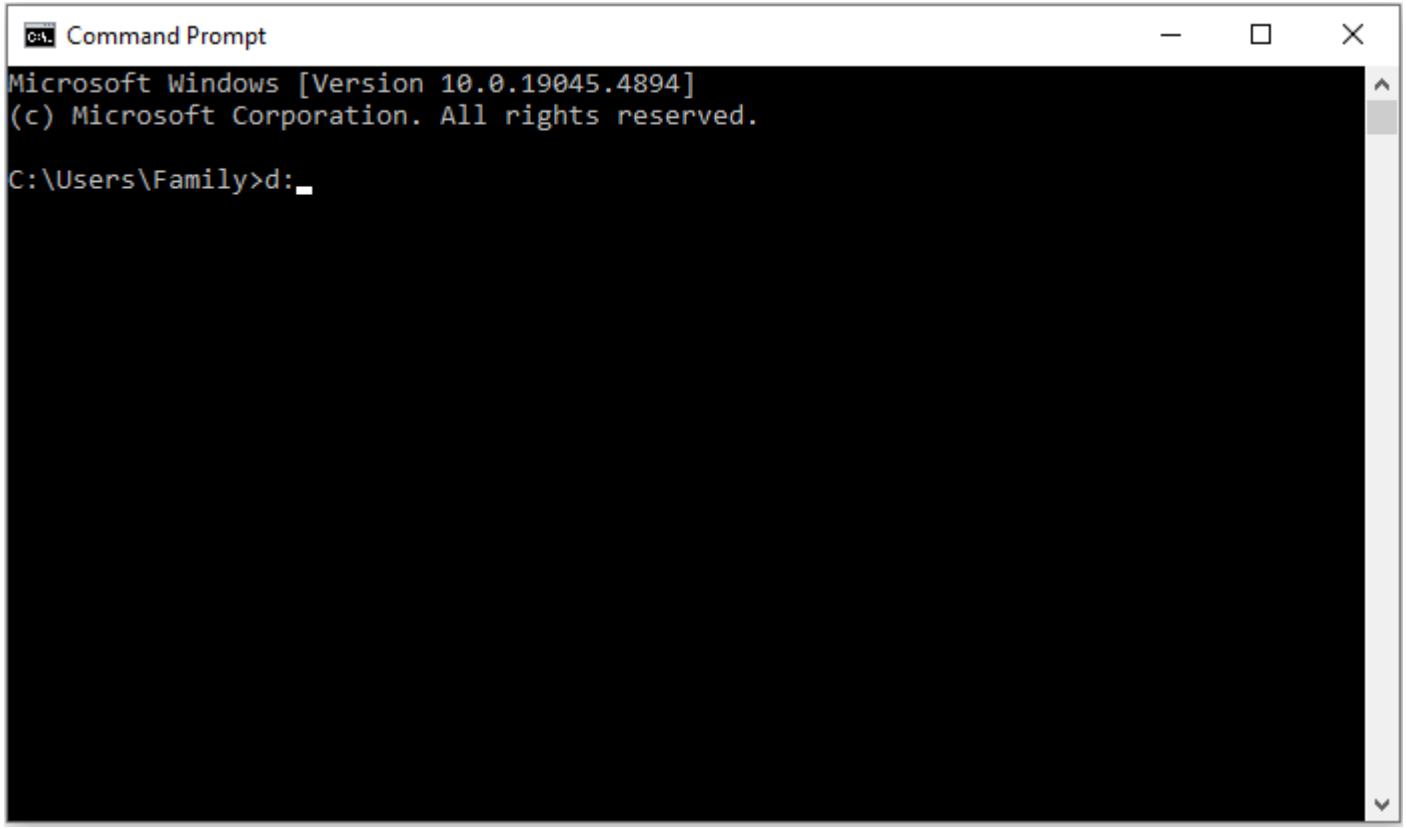
3. Video processing:
   - DPRAM can be used in video processing systems **to store and access video frames**.
     - This allows multiple processing units to *read from* and *write to* the memory *simultaneously*,
       - enabling real-time video processing.
4. Test and measurement equipment:
   - DPRAM can be used in test and measurement equipment,
     - such as **oscilloscopes** and **logic analyzers**,
       - to simultaneously capture and store data from multiple sources.
5. Medical equipment:
   - DPRAM can be used in medical equipment, such as **imaging systems**,
     - to store and process large amounts of data in real time.
   - This allows multiple circuits to access the memory simultaneously,
     - improving the speed and accuracy of the medical equipment.

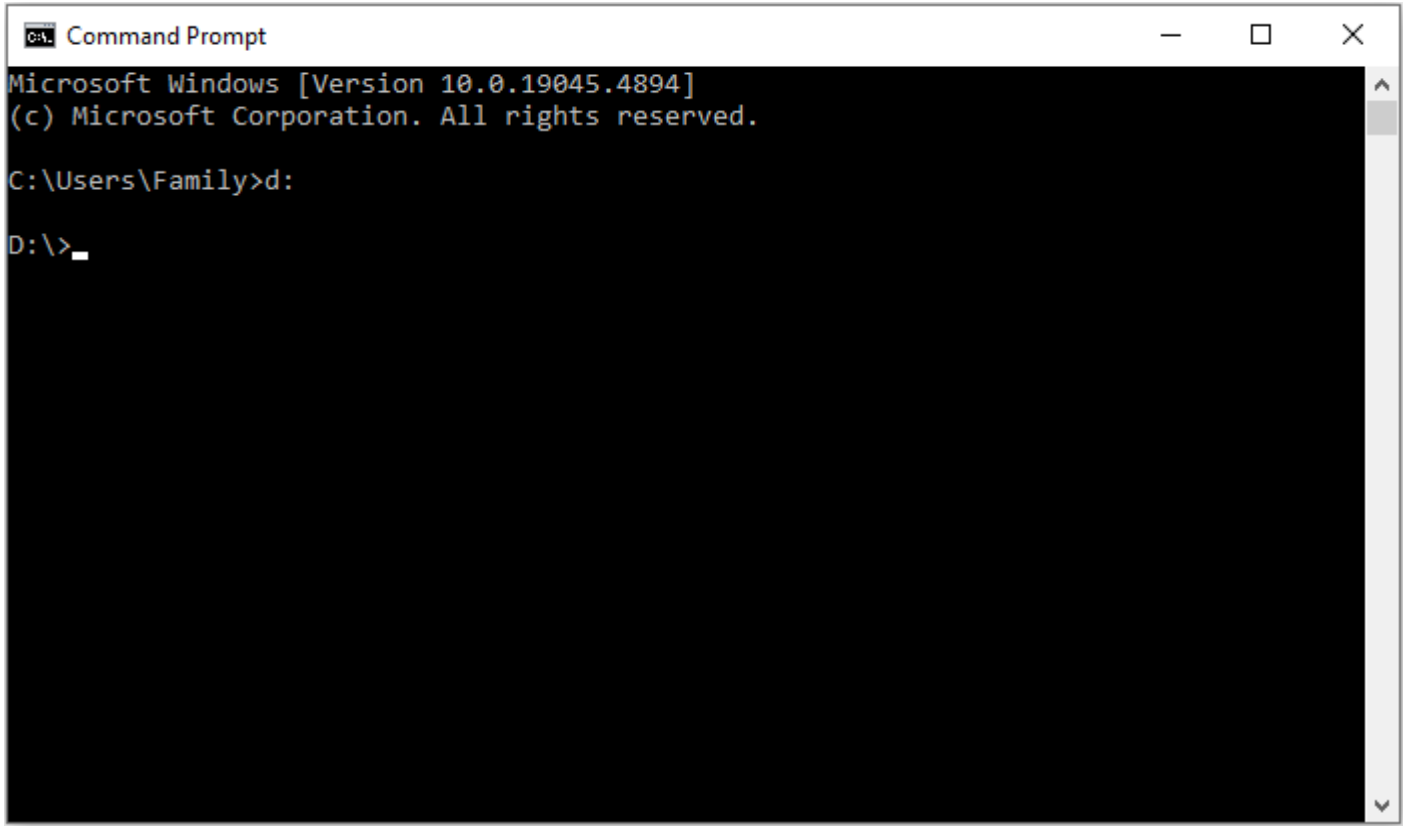
Extra Slide

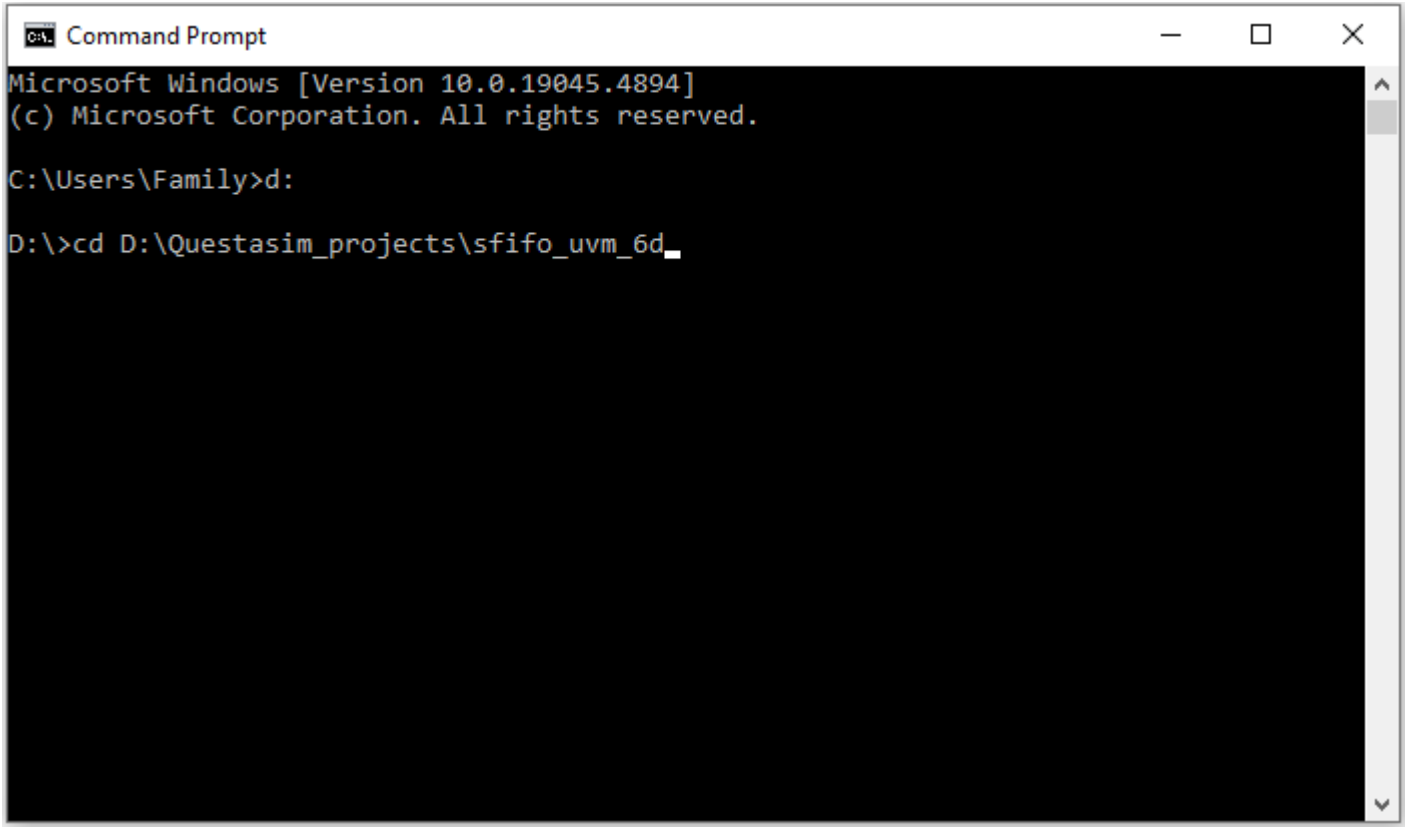
EXAMPLE DIRECTORY / FOLDER FOR SFIFO UVM USING .DO FILE

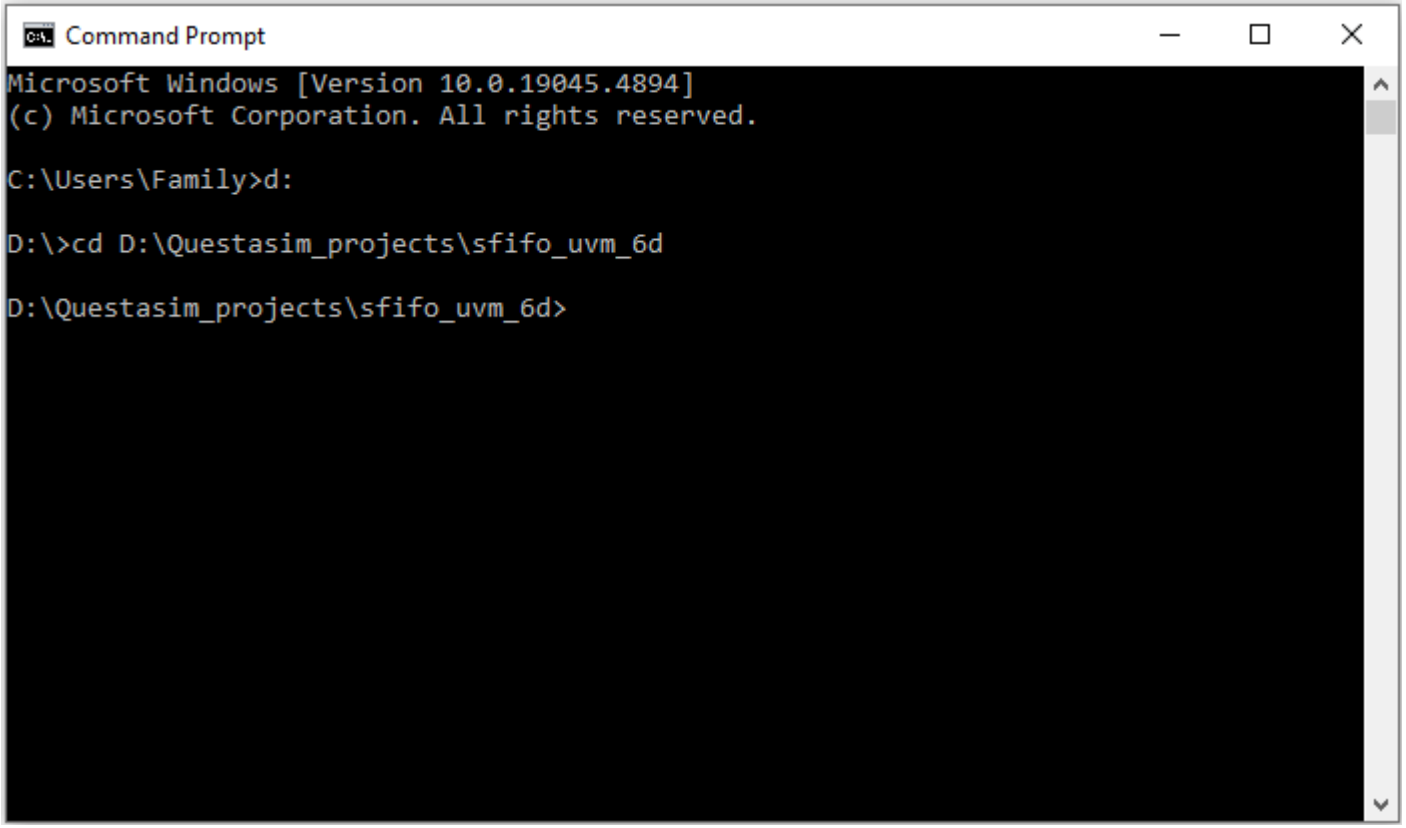

dut
sync_fifo.v
sfifo_agent.svh
sfifo_agent_pkg.sv
sfifo_driver.svh
agent
sfifo_monitor.svh
sfifo_sequencer.svh
env
sfifo_sequence_item.svh
sfifo_environment.svh
sfifo_environment_pkg.sv
sfifo_uvm
sfifo_scoreboard.svh
env_top
tb
sfifo_interface.sv
tb_top.sv
tests
seq_lib
sfifo_sequence.svh
sfifo_sequence_pkg.sv
sfifo_test.svh
sfifo_test_pkg.sv

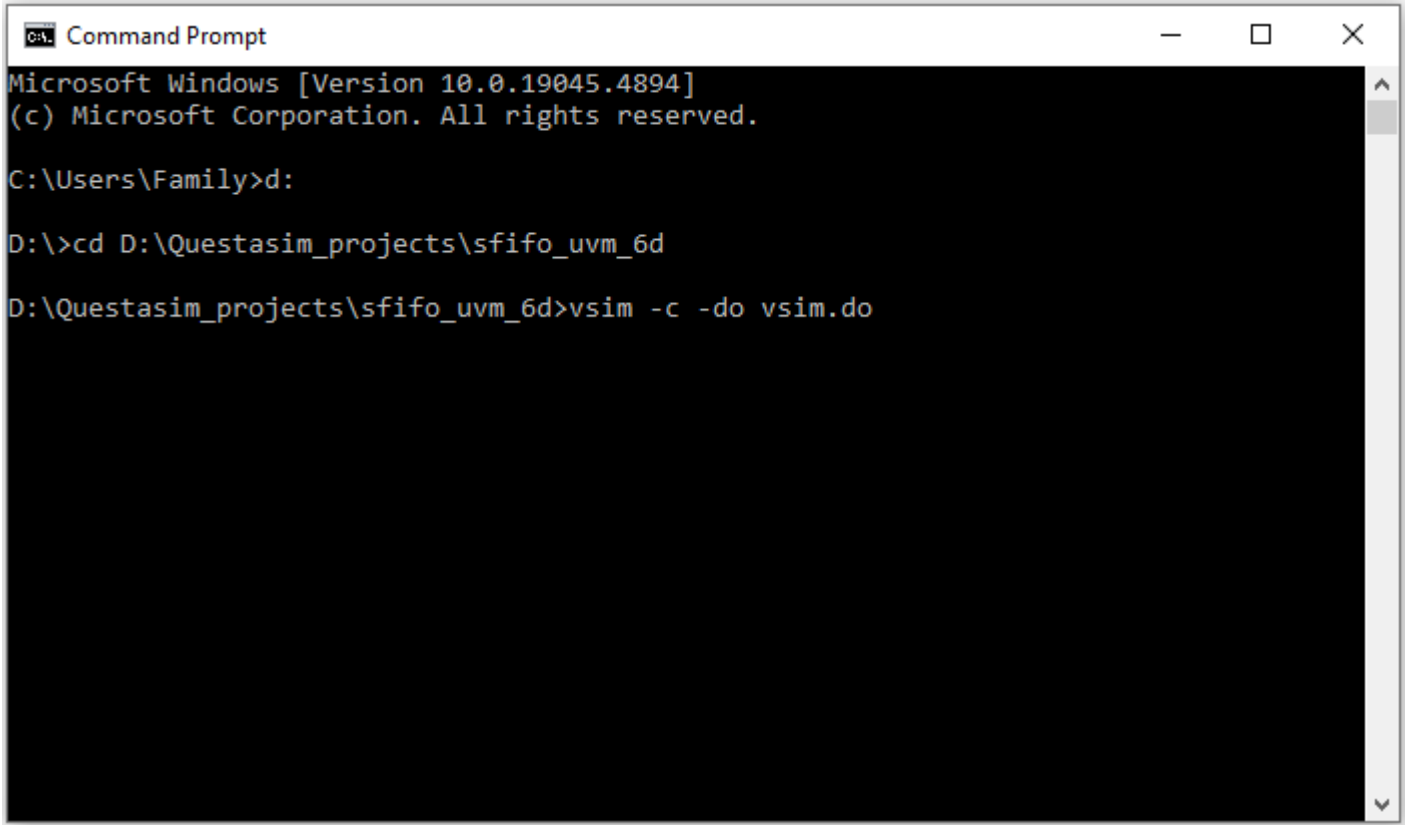

Command Prompt
Microsoft Windows [Version 10.0.19045.4894]
(c) Microsoft Corporation. All rights reserved.
C:\Users\Family>

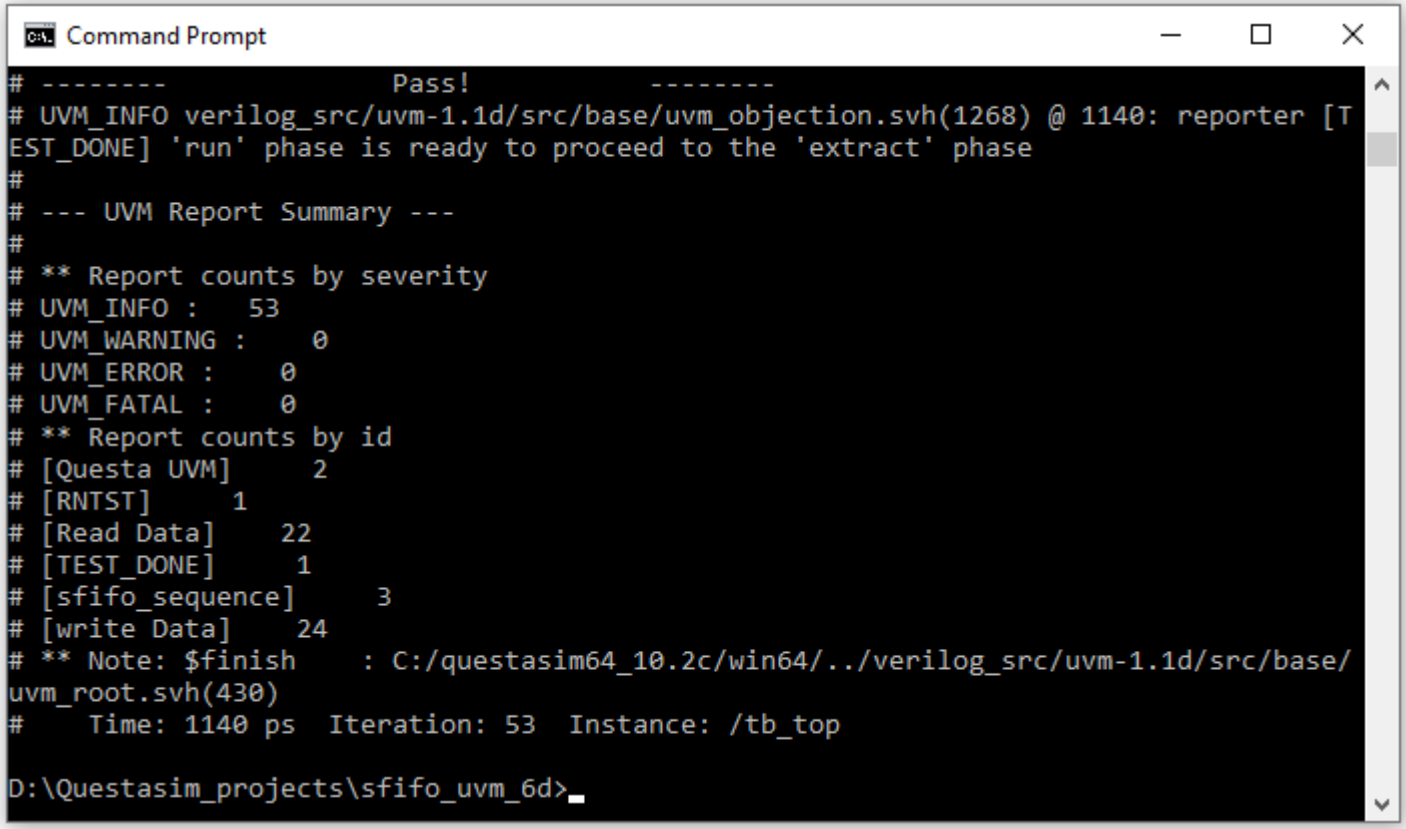

Command Prompt
Microsoft Windows [Version 10.0.19045.4894]
(c) Microsoft Corporation. All rights reserved.
C:\Users\Family>d:

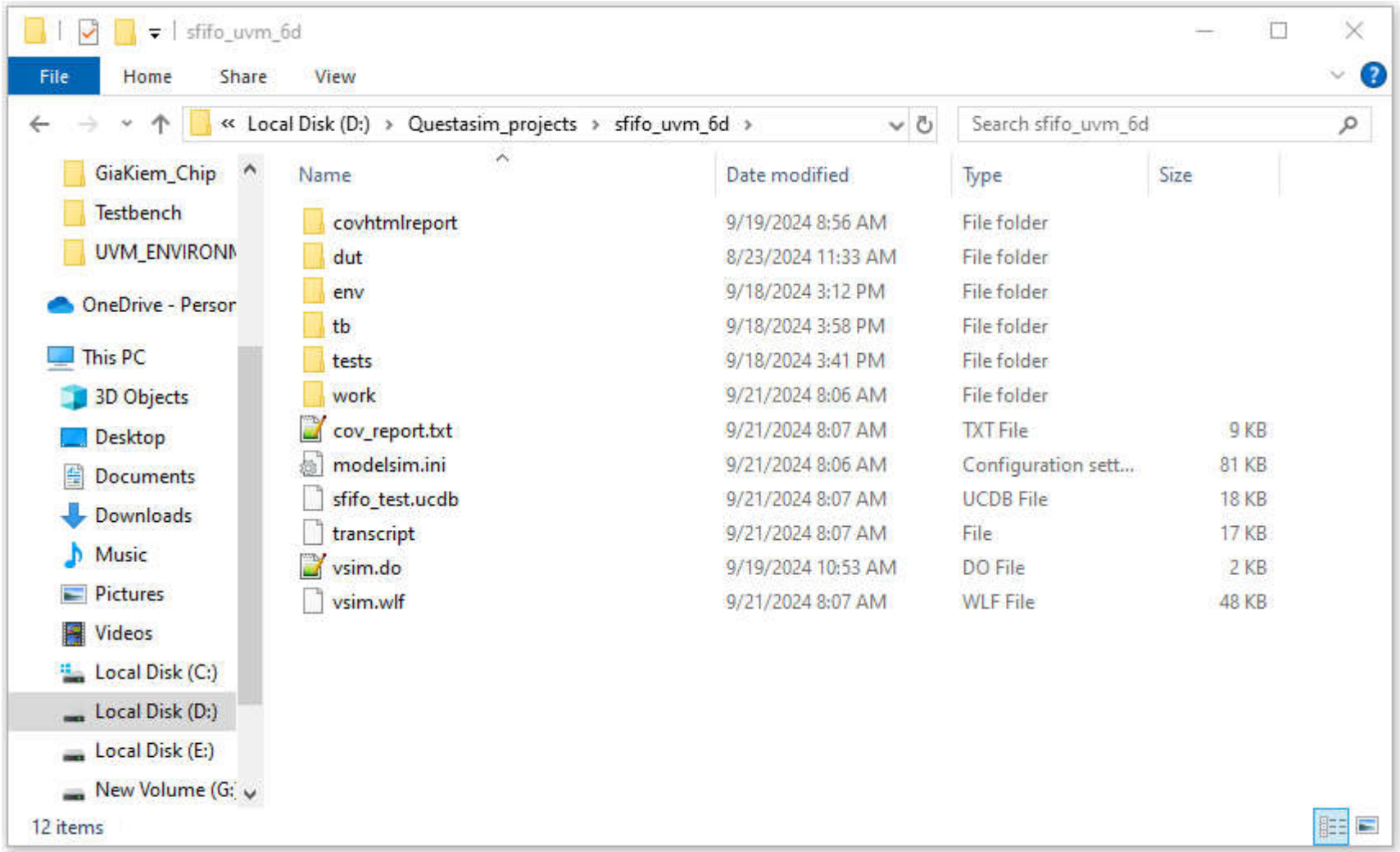

Command Prompt
Microsoft Windows [Version 10.0.19045.4894]
(c) Microsoft Corporation. All rights reserved.
C:\Users\Family>d:
D:\>


Command Prompt
Microsoft Windows [Version 10.0.19045.4894]
(c) Microsoft Corporation. All rights reserved.
C:\Users\Family>d:
D:\>cd D:\Questasim_projects\sfifo_uvm_6d


Command Prompt
Microsoft Windows [Version 10.0.19045.4894]
(c) Microsoft Corporation. All rights reserved.
C:\Users\Family>d:
D:\>cd D:\Questasim_projects\sfifo_uvm_6d
D:\Questasim_projects\sfifo_uvm_6d>


Command Prompt
Microsoft Windows [Version 10.0.19045.4894]
(c) Microsoft Corporation. All rights reserved.
C:\Users\Family>d:
D:\>cd D:\Questasim_projects\sfifo_uvm_6d
D:\Questasim_projects\sfifo_uvm_6d>vsim -c -do vsim.do


Command Prompt
--------   Pass!   --------
UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1268) @ 1140: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
#
--- UVM Report Summary ---
#
** Report counts by severity
UVM_INFO :   53
UVM_WARNING :   0
UVM_ERROR :   0
UVM_FATAL :   0
** Report counts by id
[Questa UVM]   2
[RNTST]   1
[Read Data]   22
[TEST_DONE]   1
[sfifo_sequence]   3
[write Data]   24
** Note: $finish   : C:/questasim64_10.2c/win64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
Time: 1140 ps Iteration: 53 Instance: /tb_top
D:\Questasim_projects\sfifo_uvm_6d>

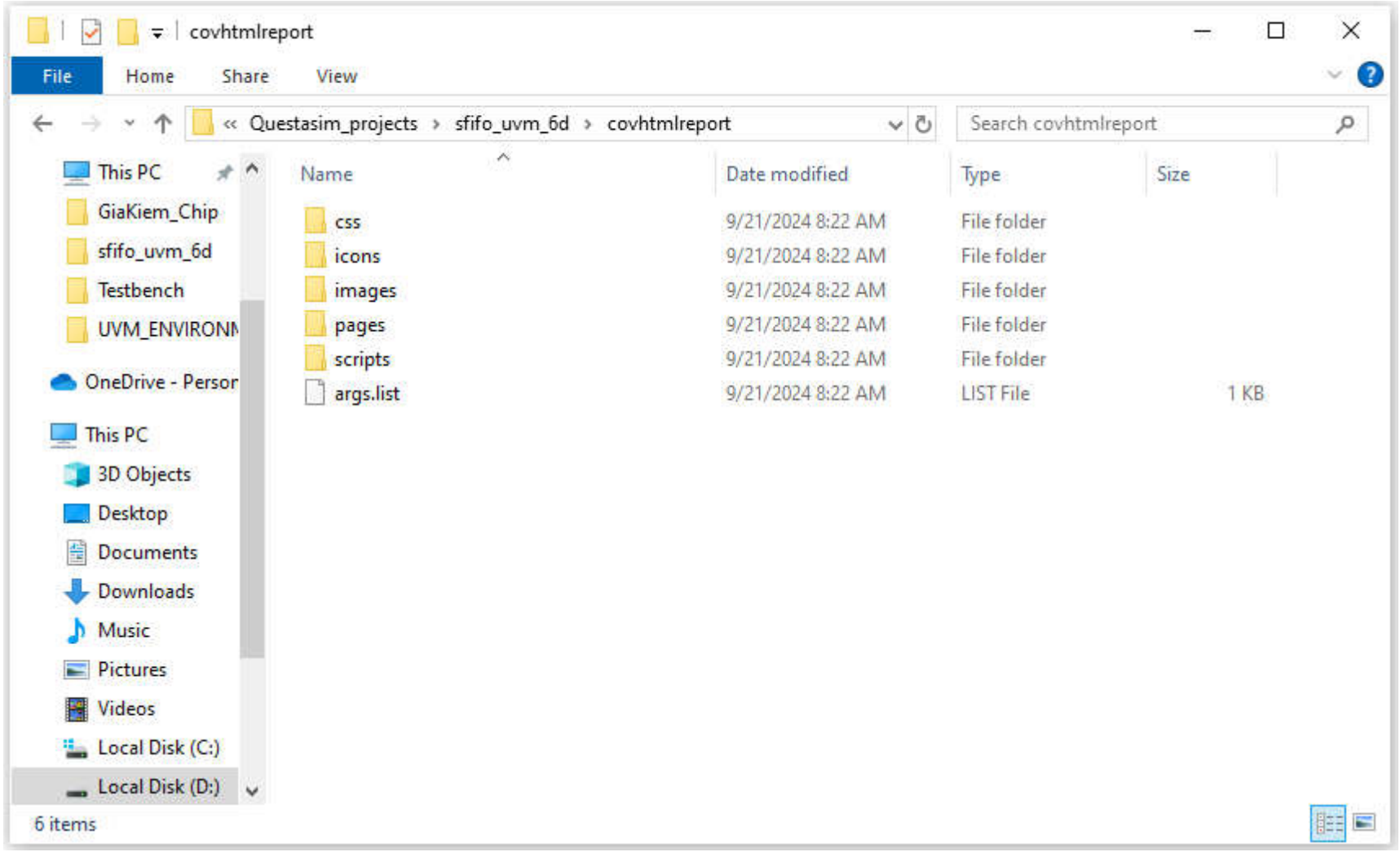

sfifo_uvm_6d
File
Home
Share
View
« Local Disk (D:) › Questasim_projects › sfifo_uvm_6d ›
Search sfifo_uvm_6d
GiaKiem_Chip
Testbench
UVM_ENVIRONM
OneDrive - Persor
This PC
3D Objects
Desktop
Documents
Downloads
Music
Pictures
Videos
Local Disk (C:)
Local Disk (D:)
Local Disk (E:)
New Volume (G:
Name
Date modified
Type
Size
covhtmlreport 9/19/2024 8:56 AM File folder
dut 8/23/2024 11:33 AM File folder
env 9/18/2024 3:12 PM File folder
tb 9/18/2024 3:58 PM File folder
tests 9/18/2024 3:41 PM File folder
work 9/21/2024 8:06 AM File folder
cov_report.txt 9/21/2024 8:07 AM TXT File 9 KB
modelsim.ini 9/21/2024 8:06 AM Configuration sett... 81 KB
sfifo_test.ucdb 9/21/2024 8:07 AM UCDB File 18 KB
transcript 9/21/2024 8:07 AM File 17 KB
vsim.do 9/19/2024 10:53 AM DO File 2 KB
vsim.wlf 9/21/2024 8:07 AM WLF File 48 KB
12 items

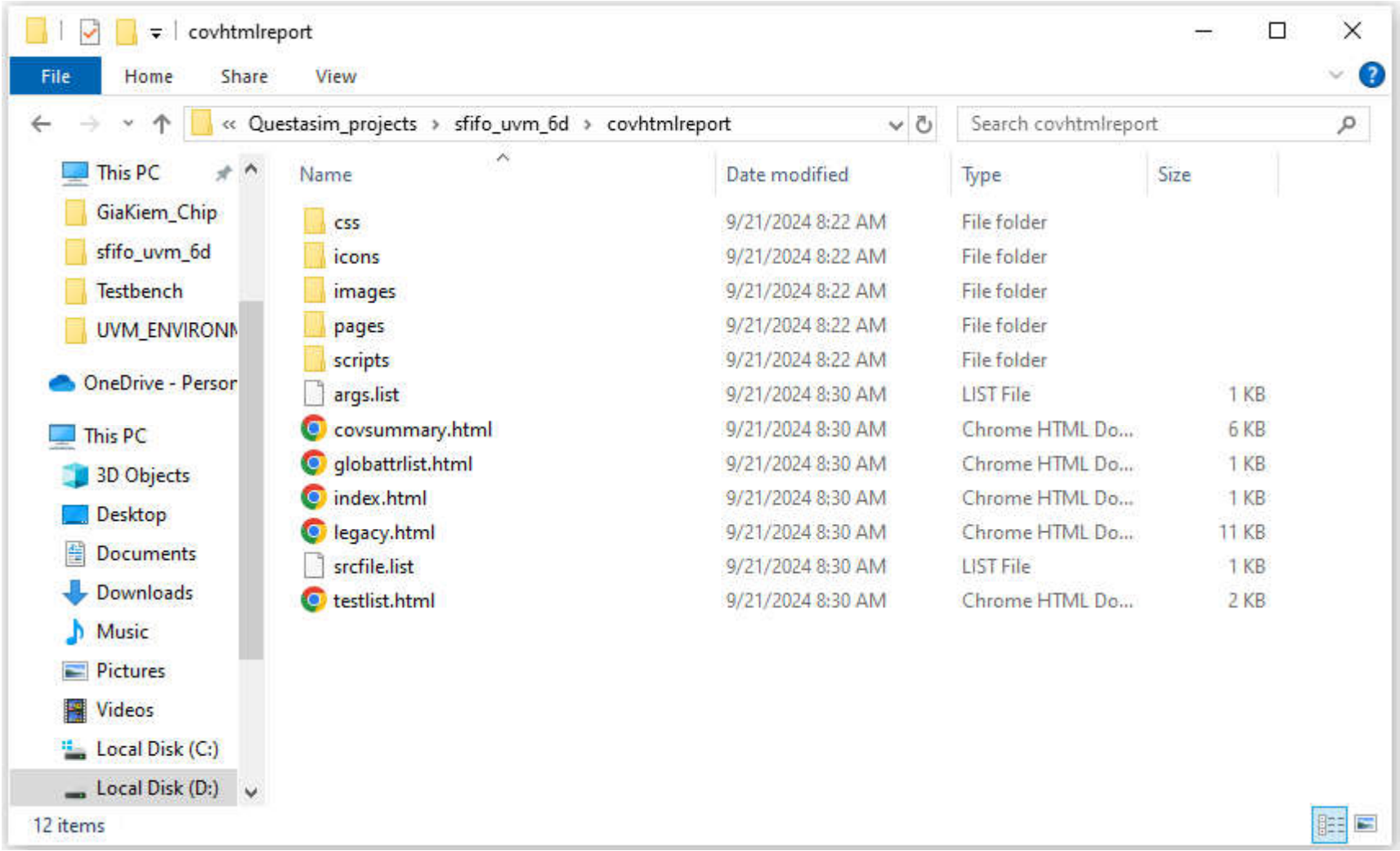
cov_report.txt

```
1  ** Error: (vcover-6805) Couldn't open file sfifo_test.ucdb in read mode.
2
```

```
Coverage Report Summary Data by file

File: ./dut/sync_fifo.v
    Enabled Coverage              Active      Hits    Misses % Covered
    ----------------              ------      ----    ------ ---------
    Stmts                             18        18         0     100.0
    Branches                           8         8         0     100.0
    FEC Condition Terms                0         0         0     100.0
    FEC Expression Terms               4         4         0     100.0
    FSMs                                                       100.0
        States                         0         0         0     100.0
        Transitions                    0         0         0     100.0

File: ./env/agent/sfifo_agent.svh
    Enabled Coverage              Active      Hits    Misses % Covered
    ----------------              ------      ----    ------ ---------
    Stmts                              9         6         3      66.6
    Branches                           4         2         2      50.0
    FEC Condition Terms                0         0         0     100.0
    FEC Expression Terms               0         0         0     100.0
    FSMs                                                       100.0
        States                         0         0         0     100.0
        Transitions                    0         0         0     100.0

File: ./env/agent/sfifo_driver.svh
    Enabled Coverage              Active      Hits    Misses % Covered
    ----------------              ------      ----    ------ ---------
    Stmts                             23        19         4      82.6
    Branches                           7         3         4      42.8
    FEC Condition Terms                0         0         0     100.0
    FEC Expression Terms               0         0         0     100.0
    FSMs                                                       100.0
        States                         0         0         0     100.0
        Transitions                    0         0         0     100.0

File: ./env/agent/sfifo_monitor.svh
    Enabled Coverage              Active      Hits    Misses % Covered
    ----------------              ------      ----    ------ ---------
    Stmts                             23        19         4      82.6
    Branches                           7         4         3      57.1
    FEC Condition Terms                0         0         0     100.0
```

html folder


covhtmlreport
File
Home
Share
View
« Questasim_projects › sfifo_uvm_6d › covhtmlreport
Search covhtmlreport
This PC
GiaKiem_Chip
sfifo_uvm_6d
Testbench
UVM_ENVIRONM
OneDrive - Persor
This PC
3D Objects
Desktop
Documents
Downloads
Music
Pictures
Videos
Local Disk (C:)
Local Disk (D:)
Name
Date modified
Type
Size
css 9/21/2024 8:22 AM File folder
icons 9/21/2024 8:22 AM File folder
images 9/21/2024 8:22 AM File folder
pages 9/21/2024 8:22 AM File folder
scripts 9/21/2024 8:22 AM File folder
args.list 9/21/2024 8:22 AM LIST File 1 KB
6 items


covhtmlreport
File
Home
Share
View
« Questasim_projects › sfifo_uvm_6d › covhtmlreport
Search covhtmlreport
This PC
GiaKiem_Chip
sfifo_uvm_6d
Testbench
UVM_ENVIRONM
OneDrive - Persor
This PC
3D Objects
Desktop
Documents
Downloads
Music
Pictures
Videos
Local Disk (C:)
Local Disk (D:)
Name
Date modified
Type
Size
css 9/21/2024 8:22 AM File folder
icons 9/21/2024 8:22 AM File folder
images 9/21/2024 8:22 AM File folder
pages 9/21/2024 8:22 AM File folder
scripts 9/21/2024 8:22 AM File folder
args.list 9/21/2024 8:30 AM LIST File 1 KB
covsummary.html 9/21/2024 8:30 AM Chrome HTML Do... 6 KB
globattrlist.html 9/21/2024 8:30 AM Chrome HTML Do... 1 KB
index.html 9/21/2024 8:30 AM Chrome HTML Do... 1 KB
legacy.html 9/21/2024 8:30 AM Chrome HTML Do... 11 KB
srcfile.list 9/21/2024 8:30 AM LIST File 1 KB
testlist.html 9/21/2024 8:30 AM Chrome HTML Do... 2 KB
12 items

Testplan | Design | DesUnits

- tb_top
  - uvm_pkg (no coverage)
  - sfifo_agent_pkg
  - sfifo_sequence_pkg
  - sfifo_environment_pkg
  - sfifo_test_pkg
  - tb_top_sv_unit (no coverage)
  - questa_uvm_pkg (no coverage)

Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

List of global attributes included in report...

Coverage Summary by Structure:

Design Scope	Coverage
tb_top	98.55%
tif	98.86%
dut	98.05%
sfifo_agent_pkg	24.86%
sfifo_seq_item	1.69%
sfifo_sequencer	25.00%
sfifo_driver	62.73%
sfifo_monitor	69.87%
sfifo_agent	58.33%
sfifo_sequence_pkg	61.37%
sfifo_sequence	61.37%
sfifo_environment_pkg	80.53%
sfifo_scoreboard	74.82%
sfifo_coverage	80.20%
sfifo_environment	70.00%
sfifo_test_pkg	81.81%
sfifo_test	81.81%

Coverage Summary by Type:

Total Coverage:					61.47%	78.92%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	20	19	1	1	95.00%	97.91%
Statements	223	132	91	1	59.19%	59.19%
Branches	126	28	98	1	22.22%	22.22%
FEC Expressions	4	4	0	1	100.00%	100.00%
Toggles	138	130	8	1	94.20%	94.20%
Assertions	3	3	0	1	100.00%	100.00%

Thank You