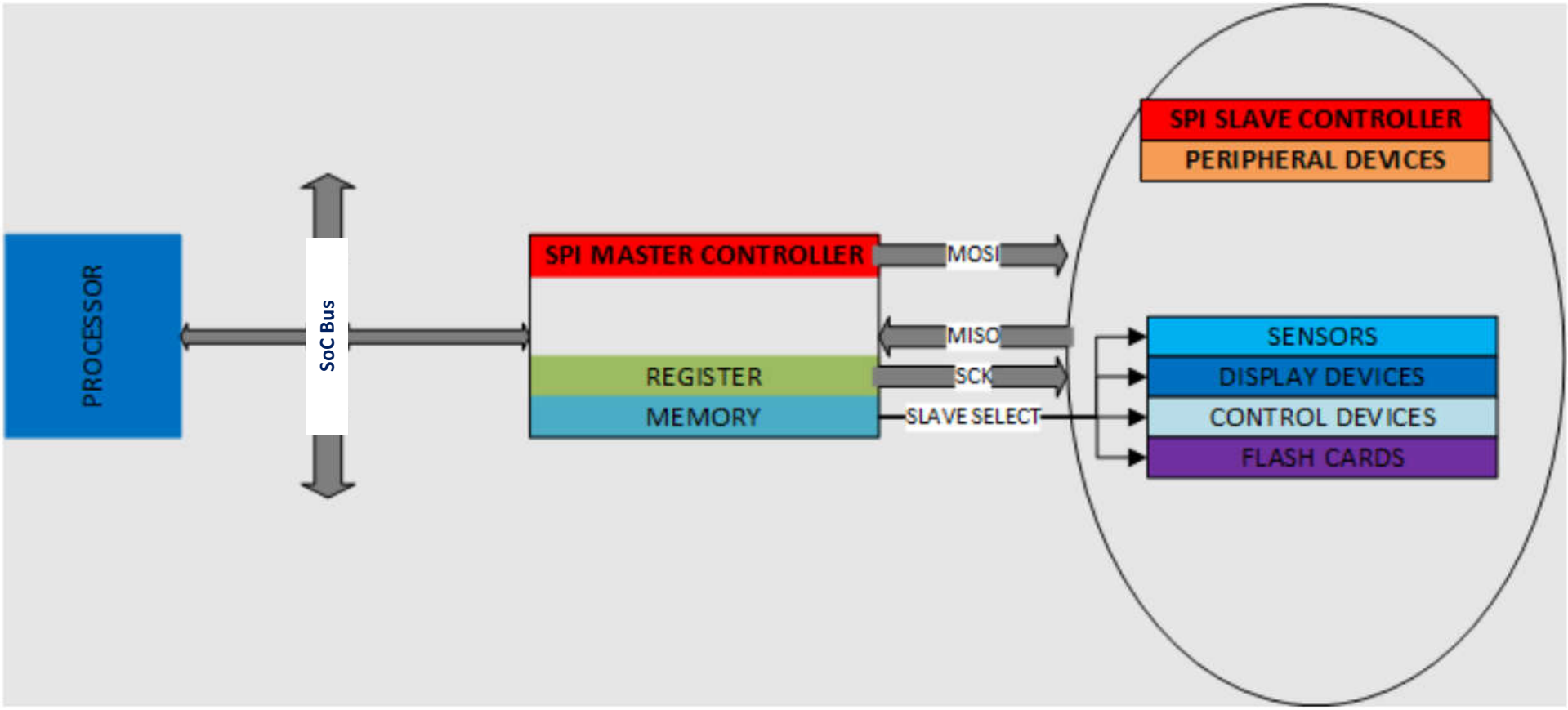
SPI Bus (Serial Peripheral Interface Bus)

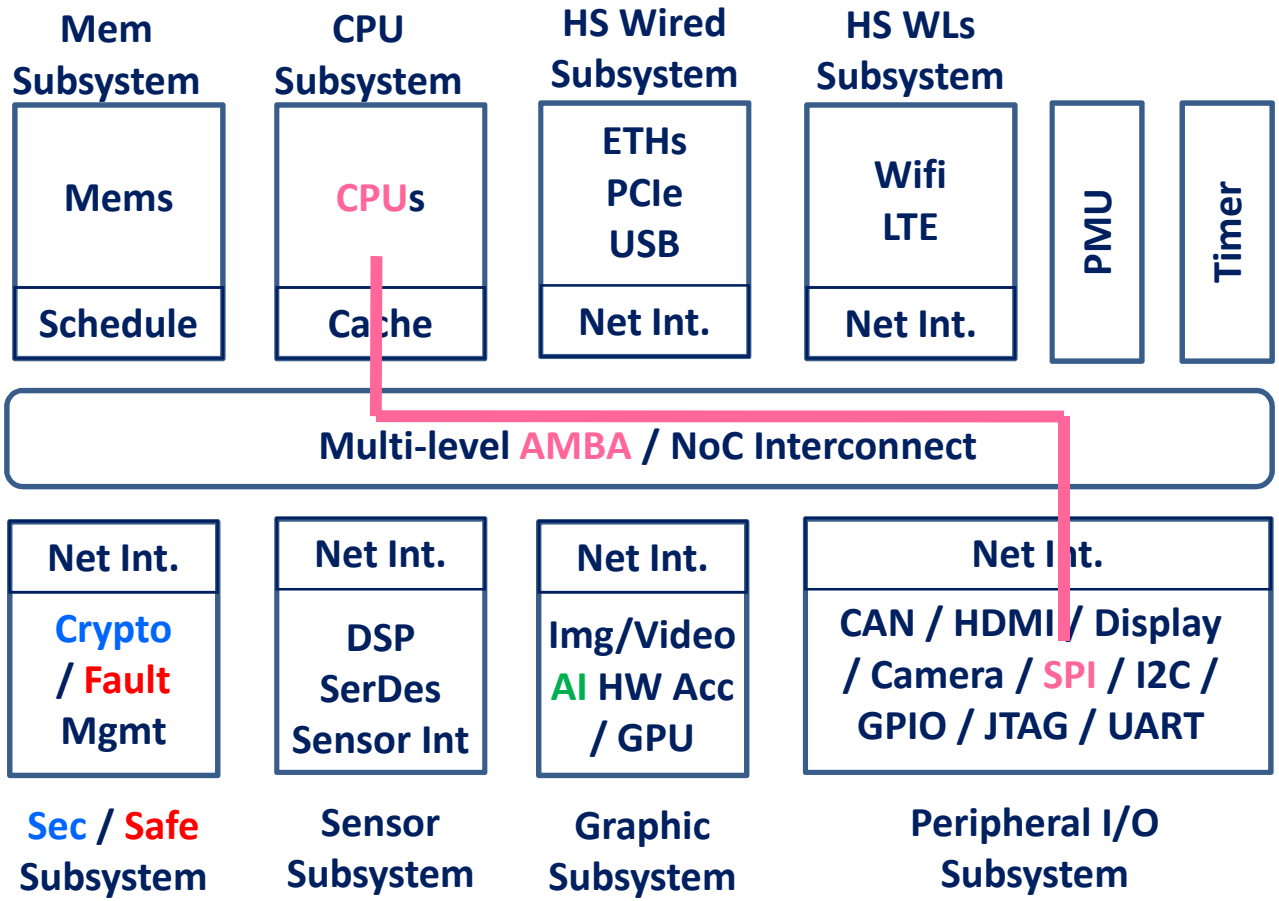
For SW Engineers

Tuan Nguyen-viet

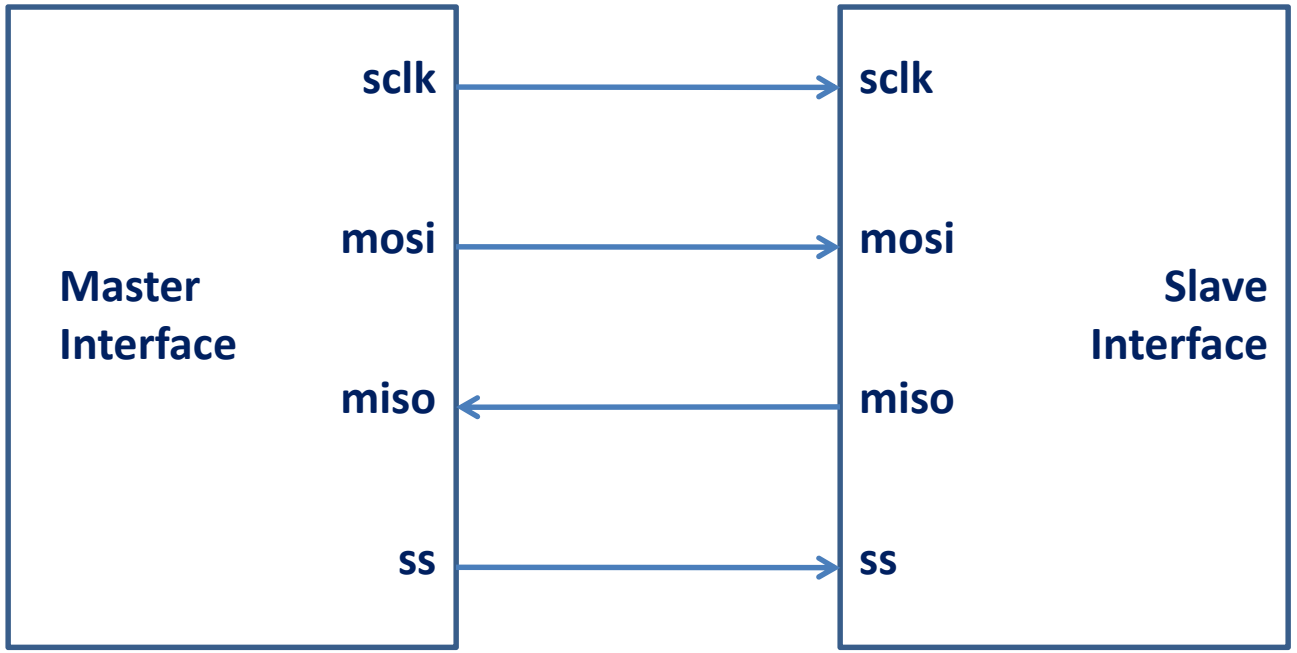
Processor-SPI Interaction



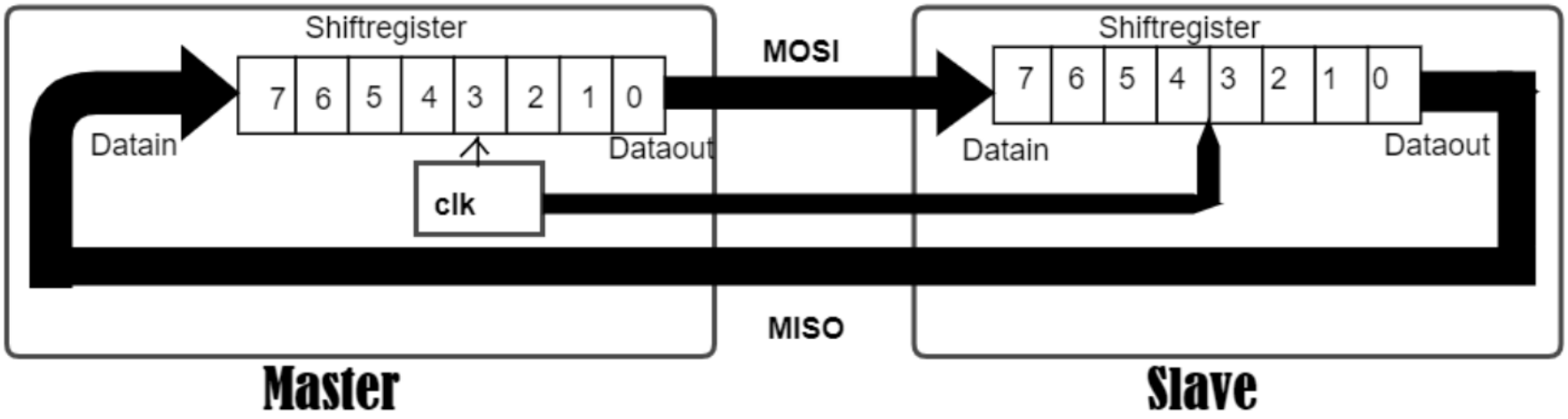
Processor-SPI Interaction (2)



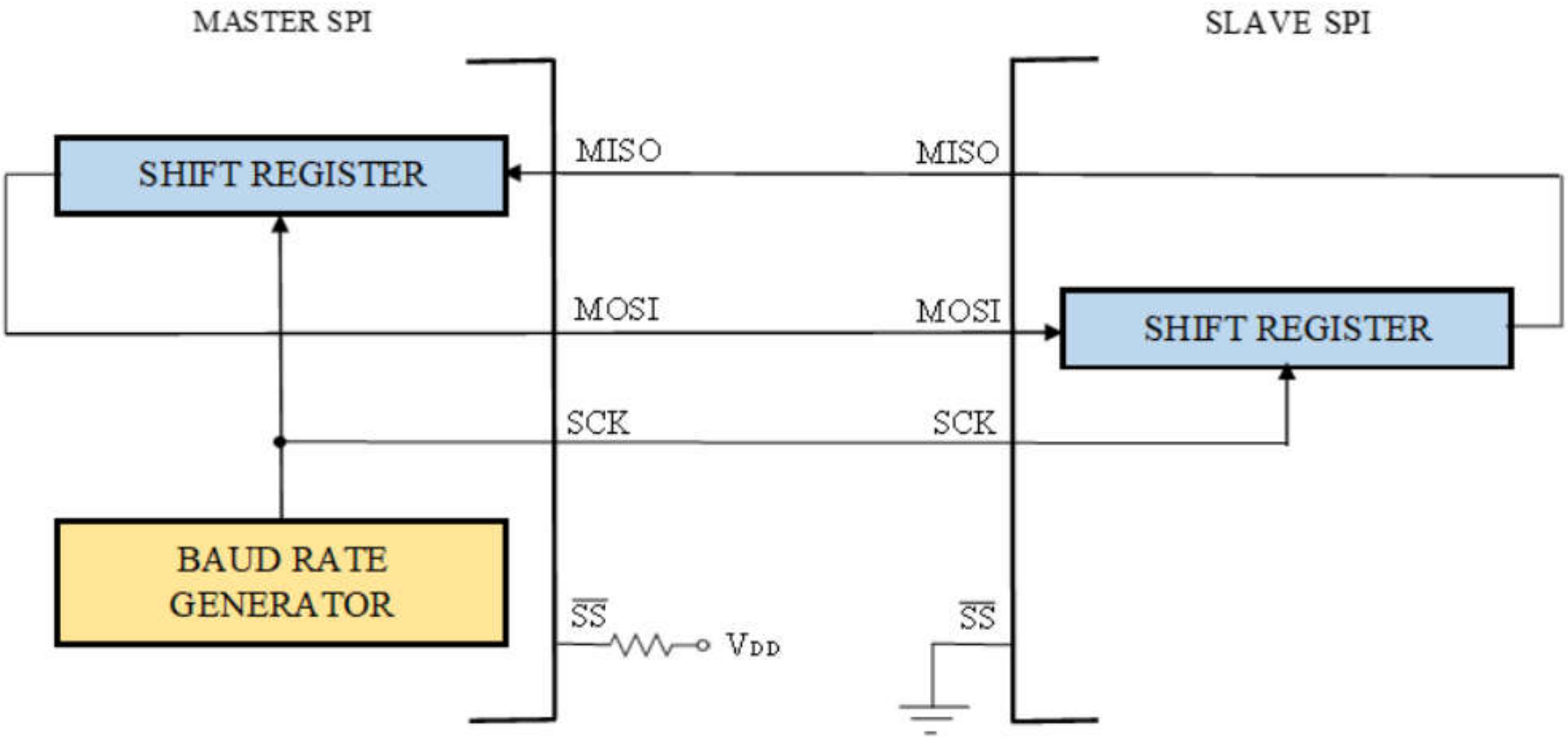
SPI Master / Slave



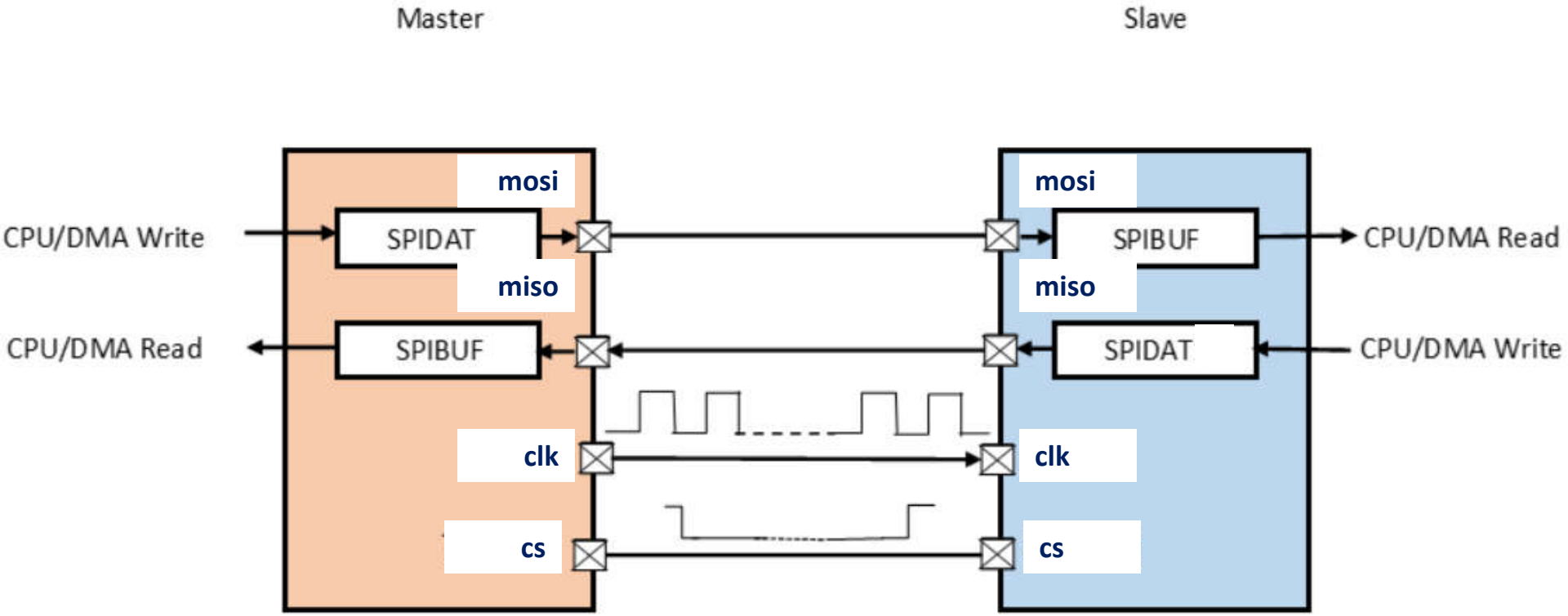
Serial 8-bit Transfer



Data Transfer b/w Master and Slave



Data Transfer b/w Master and Slave (2)



An Example of SPI Diagram

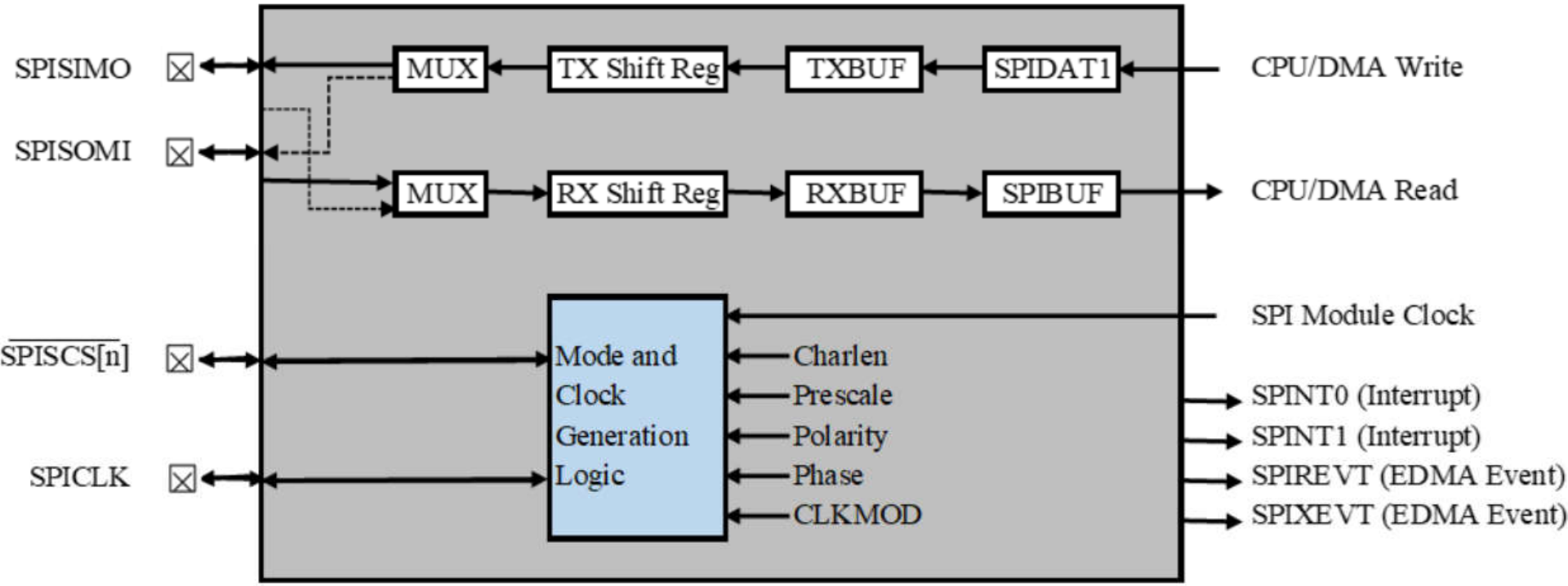
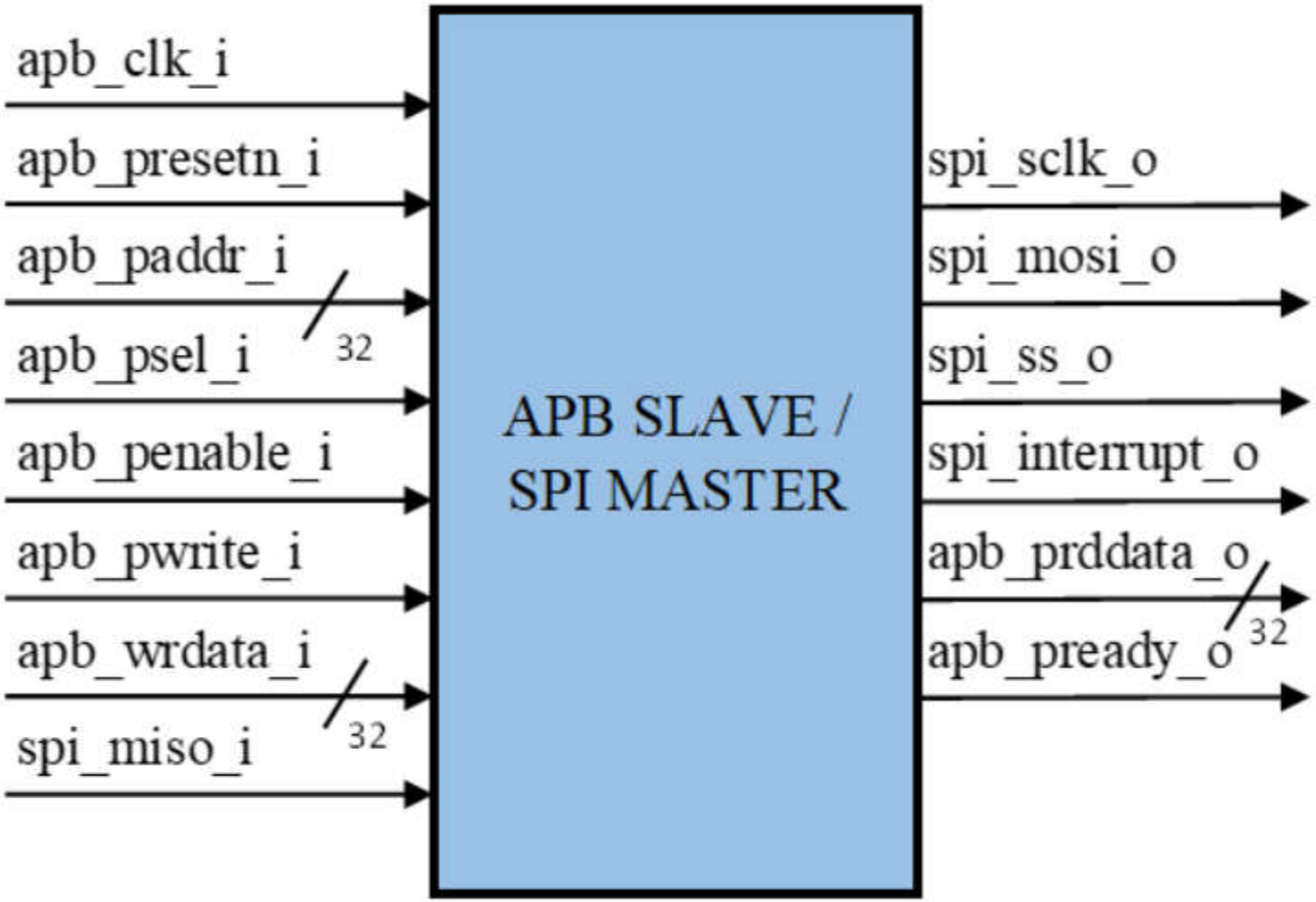
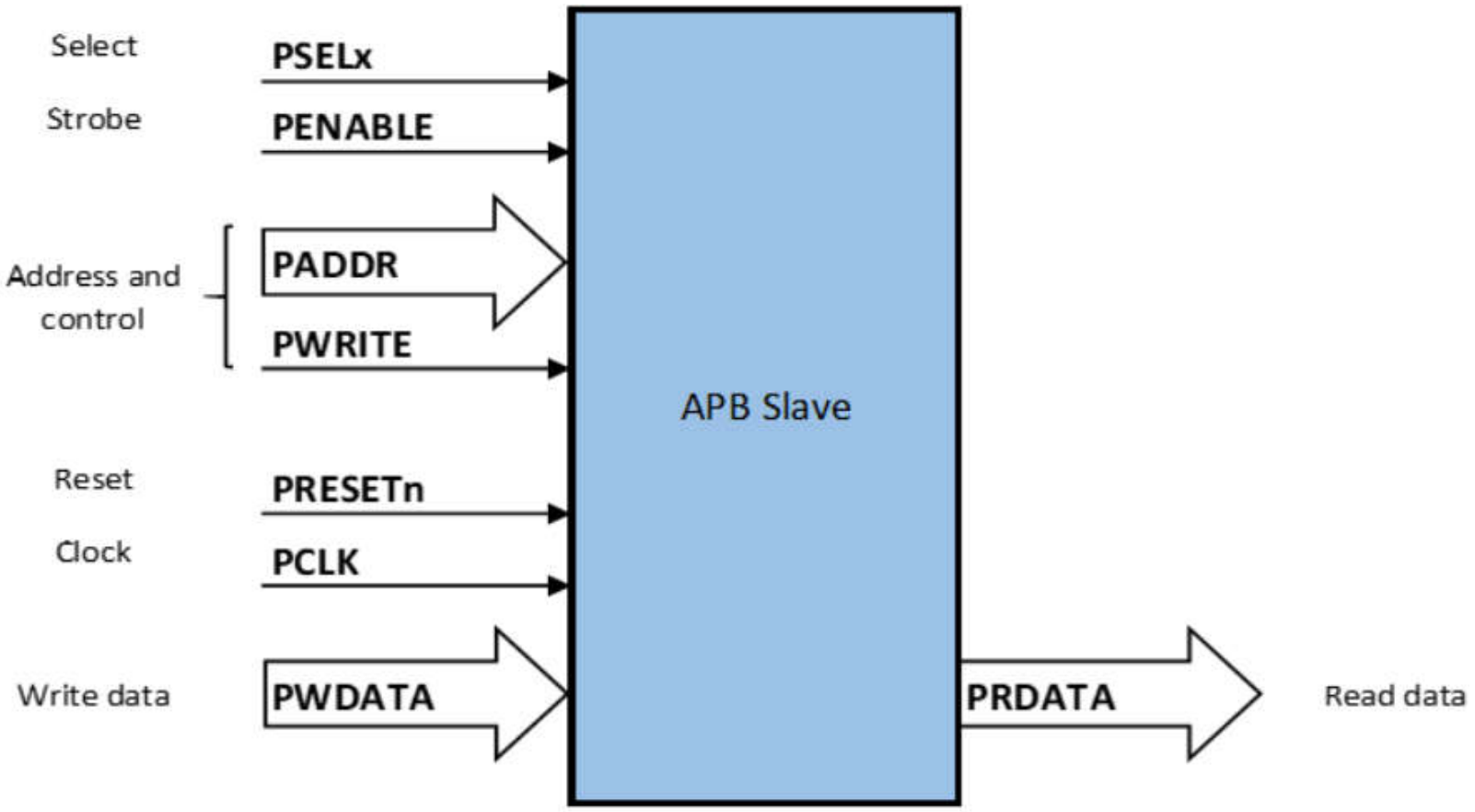


Fig. 5.1 Functional Block diagram of SPI protocol

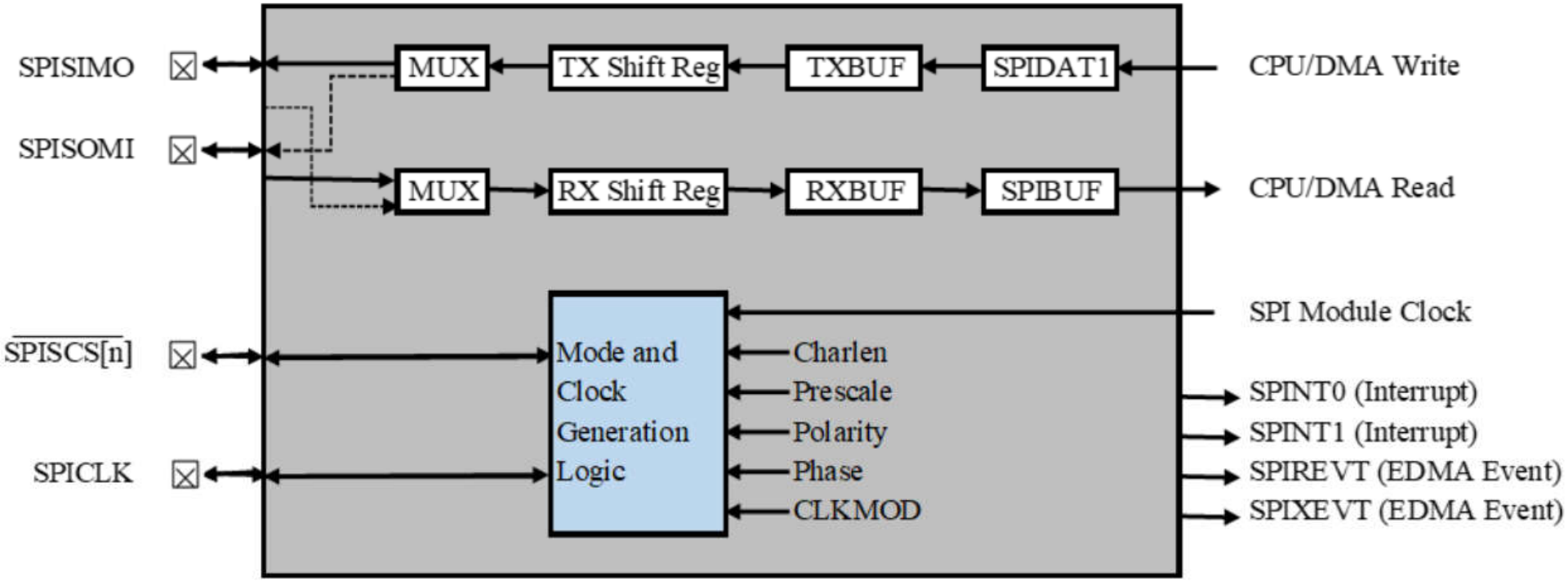
APB – SPI Interworking



An APB Slave


Select
PSELx
Strobe
PENABLE
Address and control
PADDR
PWRITE
APB Slave
Reset
PRESETn
Clock
PCLK
Write data
PWDATA
PRDATA
Read data

Functional Block diagram of SPI protocol



Wishbone Bus Interface
(Note: Academic)

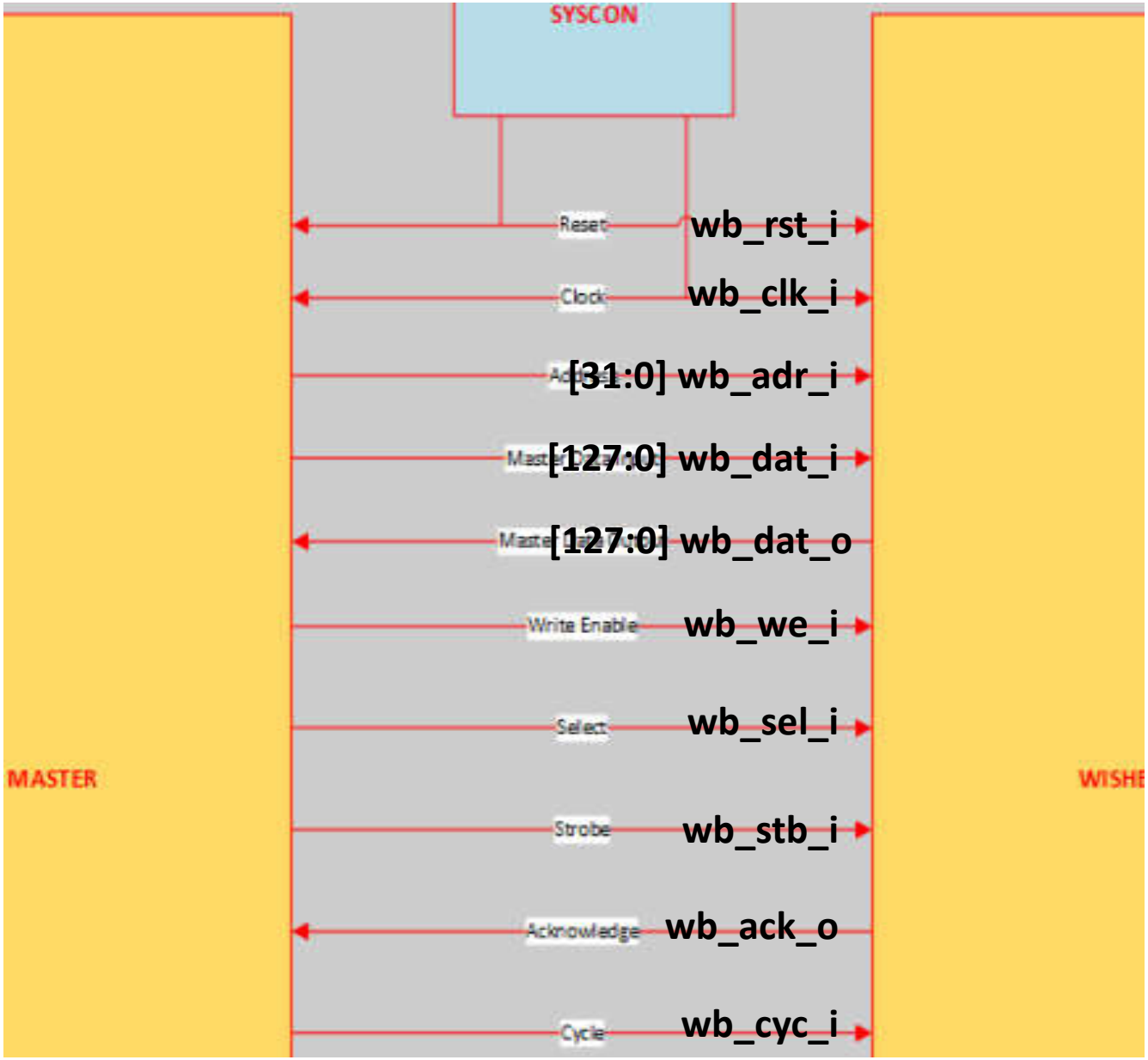
Wishbone Bus and Academic Organization

- **Wishbone bus** is used to design **SoC** system
  - because
    - it is **open source**
    - and **wishbone**-based IP's are freely provided by opencores organization.

Overview

- **Wishbone** is a flexible **SoC interconnection architecture** used with different **IP cores**.
- It enables a faster design re-usability by avoiding integration issues on a SoC.
- Wishbone interface is used as it is independent of the various logic signaling levels of different **IP cores on a chip**.
- It employs a simple Master-Slave architecture like the SPI which makes the design interface easier.
- Wishbone also employs parallel communication between devices which results in faster execution.

Wishbone Interface



Wishbone - SPI

- **Wishbone Master** is considered as **the host** to the SPI.
- It implies that **SPI master** device is a *Wishbone compliant* **slave device**.
- The **Wishbone signals** used in interfacing with the SPI are tabulated in Table below.

Table 4.3: Wishbone Signals[1, 5]

Signal	Width	Direction	Description
wb_clk_i	1	Input	System Clock
wb_rst_i	1	Input	Active high synchronous Reset
wb_adr_i	32	Input	Address
wb_dat_i	128	Input	Data to Core
wb_dat_o	128	Output	Data from Core
wb_sel_i	16	Input	Byte Select
wb_we_i	1	Input	Write Enable
wb_stb_i	1	Input	Strobe
wb_cyc_i	1	Input	Bus cycle
wb_ack_o	1	Output	Bus cycle acknowledge
wb_err_o	1	Output	Bus cycle error
wb_int_o	1	Output	Interrupt

Thank You