

Automating Simulation

REF: ModelSim® Tutorial
Software Version 10.4c

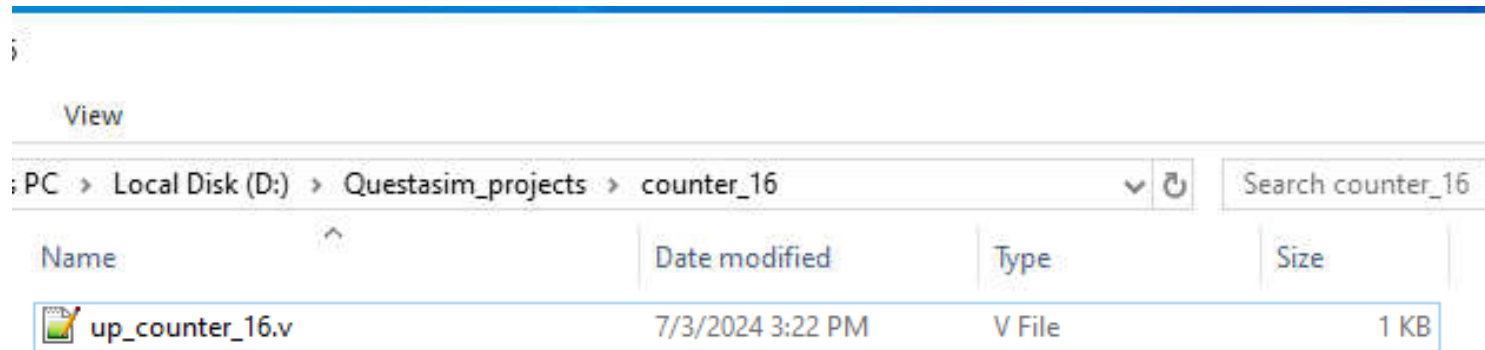
Simulation using **DO** File

Creating a Simple DO File

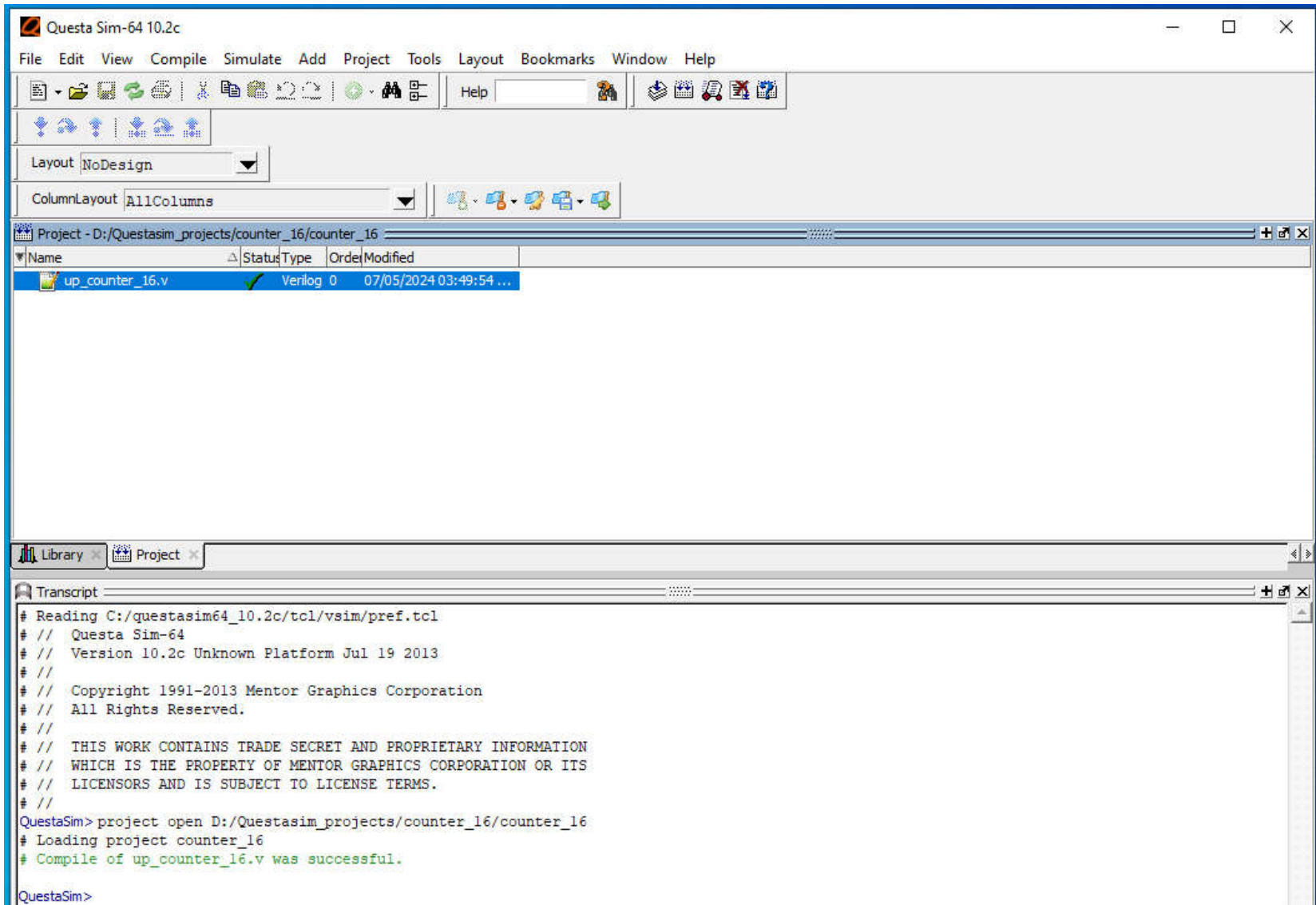
- Creating a **DO file** is as simple as typing a set of commands in a **text file**.
- We will create a **DO file** that
 - loads a design,
 - adds signals to the Wave window,
 - provides stimulus to those signals,
 - and then advances the simulation.

Create a new directory and copy the design file into it

- E.g., create **counter_16** directory/folder and copy **up_counter_16.v** into it.



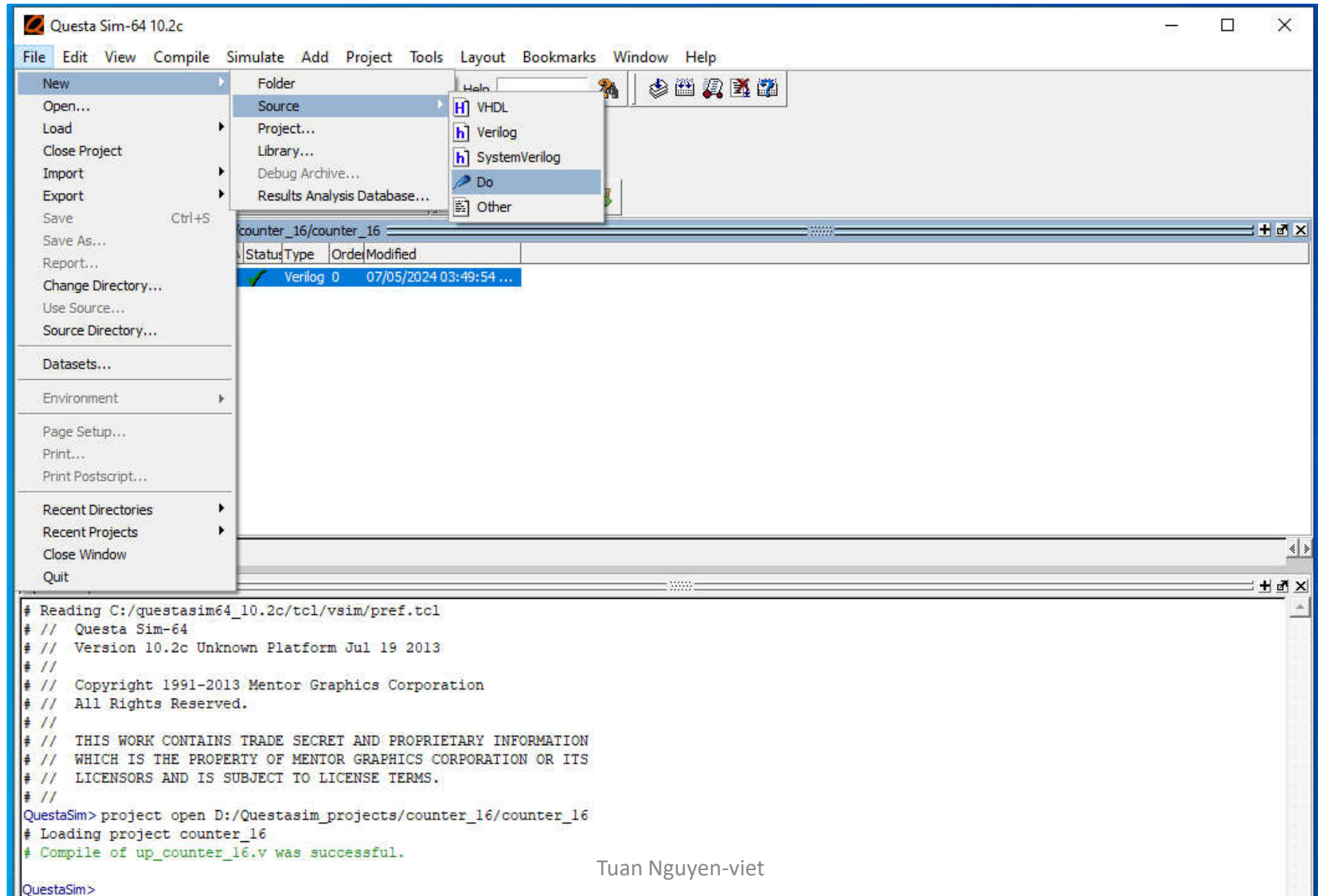
Create New Project / Add file / Compile as below



Create a **DO** file

- Create a **DO file** that will
 - add signals to the **Wave** window,
 - force signals,
 - and run the simulation.

Select **File > New > Source > Do** to create a new DO file.



A window for DO file on RHS as below

The screenshot displays the Questa Sim-64 10.2c software interface. The main window is titled "Questa Sim-64 10.2c" and features a menu bar (File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, Bookmarks, Window, Help) and a toolbar. Below the toolbar, there are several panels:

- Layout:** Set to "NoDesign".
- ColumnLayout:** Set to "AllColumns".
- Project Window:** Displays a list of files in the project "D:/Questasim_projects/counter_16/counter_16". The file "up_counter_16.v" is highlighted, showing its status as "Verilog 0" and a modification date of "07/05/2024 03:49:54 ...".
- DO File Editor:** The right-hand pane shows the content of the selected DO file, "D:/Questasim_projects/counter_16/Untitled-1.do - Default". It contains a single line of text: "1".
- Transcript Window:** The bottom pane shows the output of the simulation. It includes the following text:

```
# Reading C:/questasim64_10.2c/tcl/vsim/pref.tcl
# // Questa Sim-64
# // Version 10.2c Unknown Platform Jul 19 2013
# //
# // Copyright 1991-2013 Mentor Graphics Corporation
# // All Rights Reserved.
# //
# // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
# // WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
# // LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //
QuestaSim> project open D:/Questasim_projects/counter_16/counter_16
# Loading project counter_16
# Compile of up_counter_16.v was successful.
```

The interface is designed for simulating digital logic designs, and the DO file editor allows for the creation and modification of simulation scripts.

Enter the following commands into the window

The screenshot displays the Questa Sim-64 10.2c software interface. The main window is titled "D:/Questasim_projects/counter_16/Untitled-1.do - Default *". The interface includes a menu bar (File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, Bookmarks, Window, Help) and a toolbar with various icons. Below the toolbar, there are dropdown menus for "Layout" (set to "NoDesign") and "ColumnLayout" (set to "AllColumns").

The "Project" window on the left shows a list of files in the project "D:/Questasim_projects/counter_16/counter_16". The file "up_counter_16.v" is listed with a status of "Verilog 0" and a modification date of "07/05/2024 03:49:54...".

The main editor window contains the following Verilog commands:

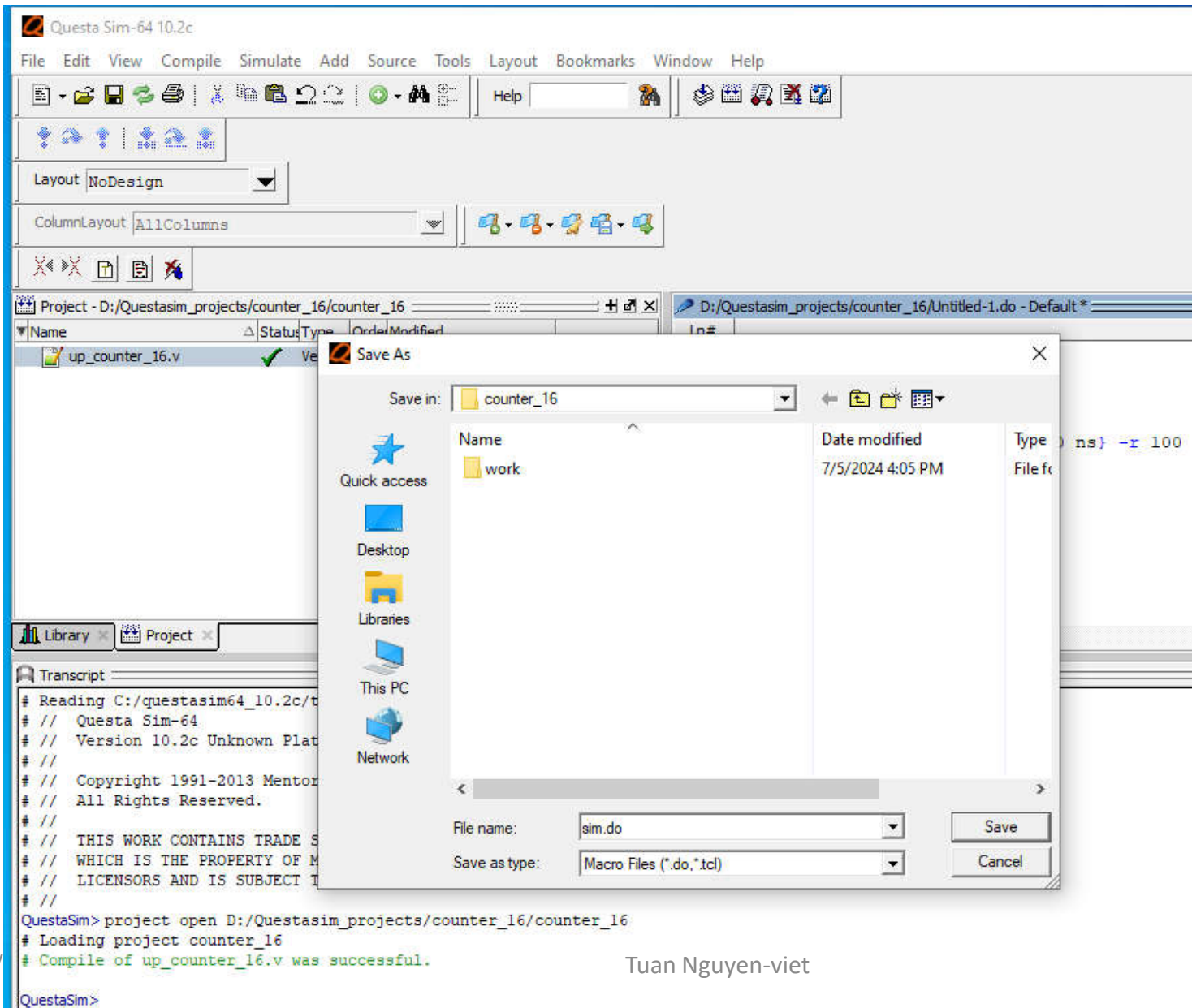
```
1 vsim up_counter_16
2 add wave out
3 add wave clock
4 add wave reset
5 force -freeze clock 0 0, 1 {50 ns} -r 100
6 force reset 1
7 run 100
8 force reset 0
9 run 300
10 force reset 1
11 run 400
12 force reset 0
13 run 200
```

The "Transcript" window at the bottom shows the output of the simulation setup:

```
# Reading C:/questasim64_10.2c/tcl/vsim/pref.tcl
# // Questa Sim-64
# // Version 10.2c Unknown Platform Jul 19 2013
# //
# // Copyright 1991-2013 Mentor Graphics Corporation
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# // WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
# // LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //
QuestaSim>project open D:/Questasim_projects/counter_16/counter_16
# Loading project counter_16
# Compile of up_counter_16.v was successful.

QuestaSim>
```





Select File > Save As / Name sim.do / Save it



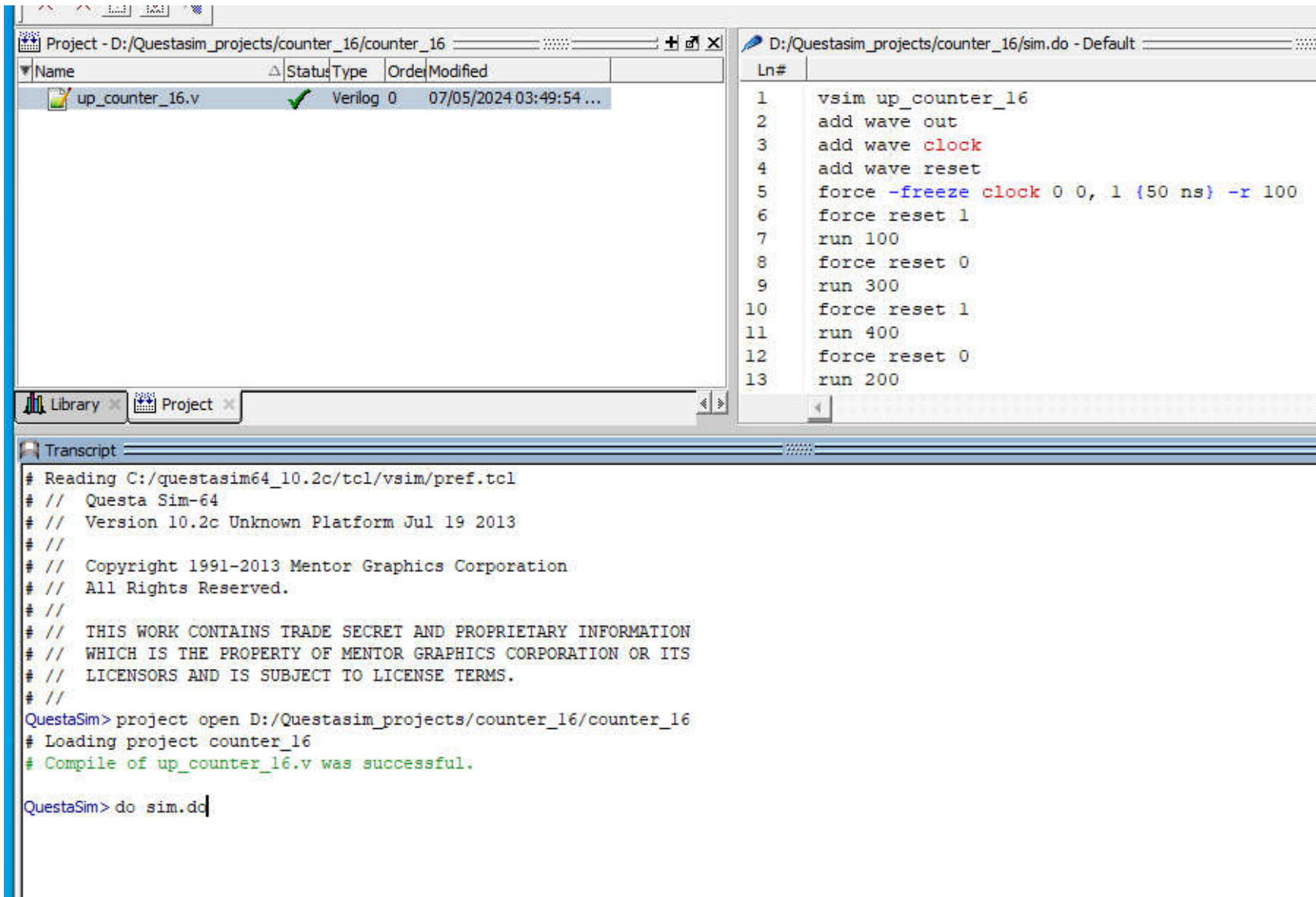
sim.do in the project directory

View

PC > Local Disk (D:) > Questasim_projects > counter_16

Name	Date modified	Type
 work	7/3/2024 9:24 PM	File folder
 sim.do	7/3/2024 10:08 PM	DO File
 transcript	7/3/2024 10:01 PM	File
 up_counter_16.v	7/3/2024 3:22 PM	V File

Enter `do sim.do` at the **QuestaSim>** prompt to execute



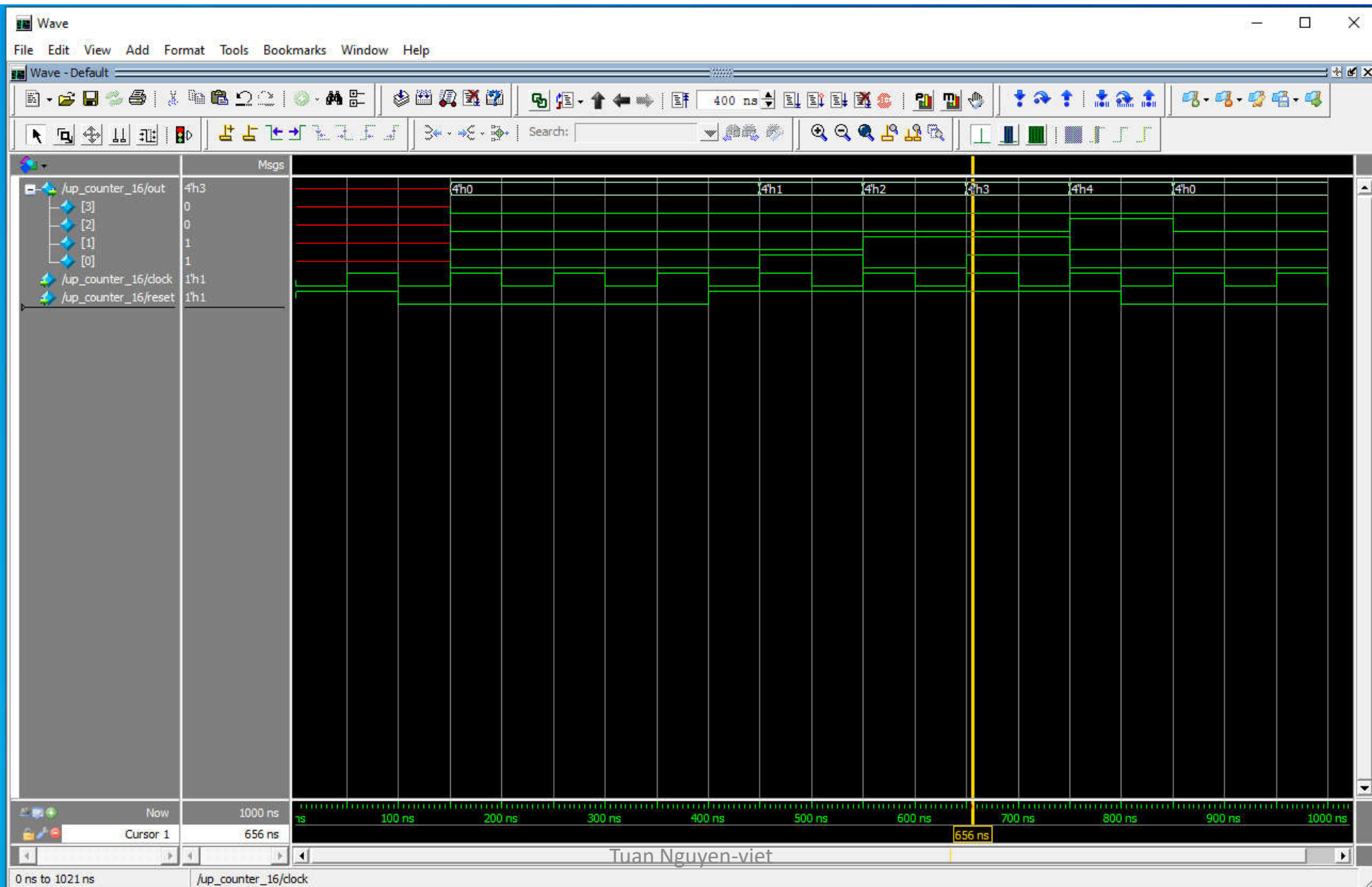
Sim automatically run

The screenshot displays the Questa Sim-64 10.2c software interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Wave, Tools, Layout, Bookmarks, Window, and Help. Below the menu bar is a toolbar with various icons for file operations, simulation control, and layout management. The main workspace is divided into several panes:

- Objects:** A tree view showing the hierarchy of the simulation. The selected object is `up_counter_16`, which has sub-objects `dock`, `reset`, and `out`.
- Wave - Default:** A waveform viewer showing the simulation results. The selected signal is `/up_counter_16/out`, which is a 4-bit bus. The waveform shows the output of the counter over time, with a cursor positioned at 656 ns.
- Transcript:** A text area at the bottom showing the simulation log. The log includes the version number (10.2c), the platform (UNKNOWN PLATFORM), the date (JUL 19 2013), and the copyright information (Copyright 1991-2013 Mentor Graphics Corporation).

The waveform viewer shows a 4-bit bus output, with the signal changing from 0 to 1 at 656 ns. The time scale is set to 500 ns, and the total simulation time is 1000 ns.

Wave window after running the DO file



Thank You