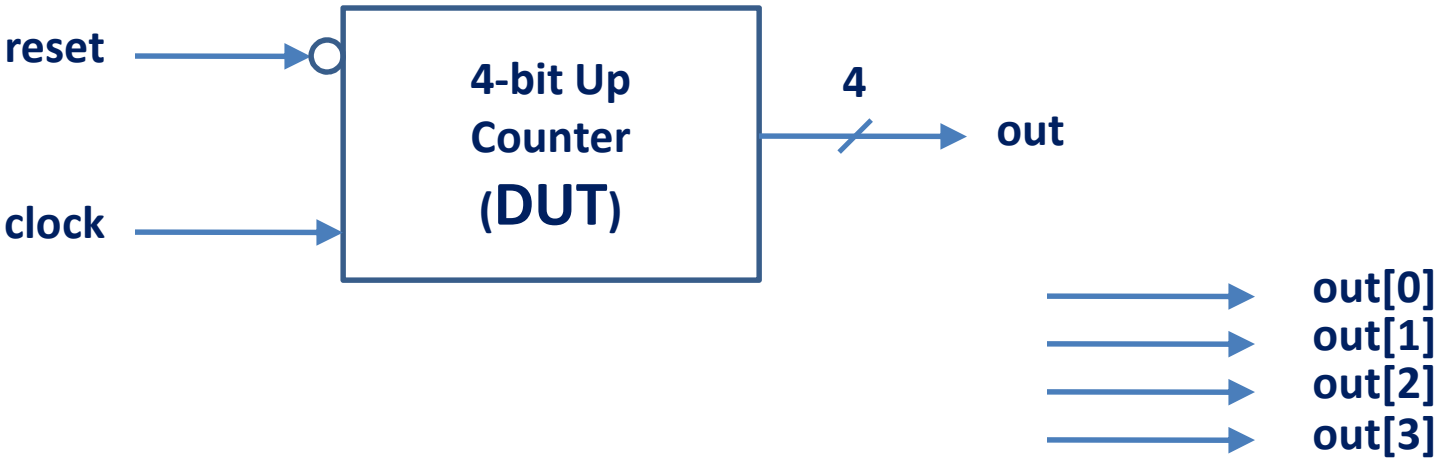
Questasim Tutorial (GUI/Windows) Continued

REF: **ModelSim® Tutorial**
Software Version 10.4c

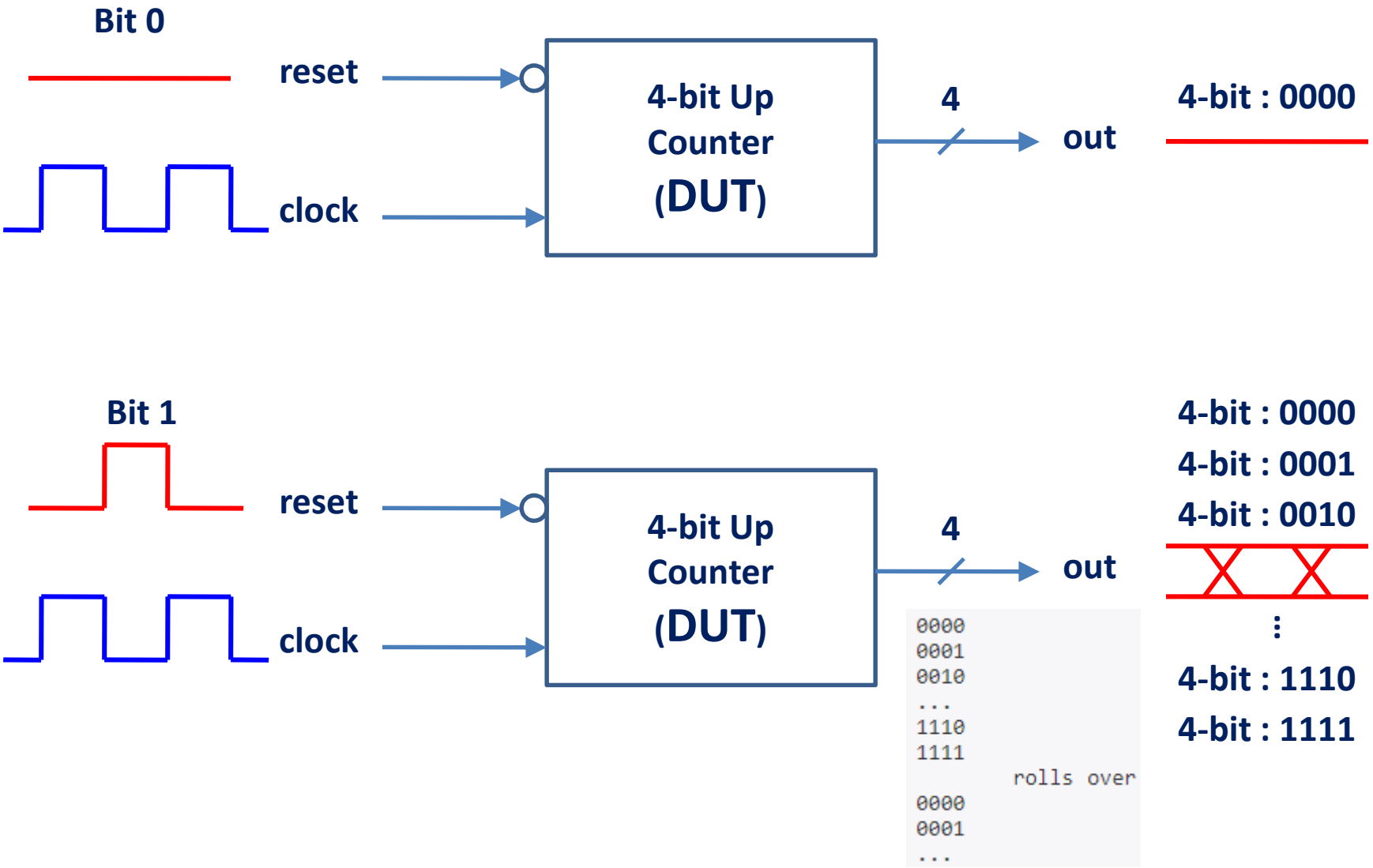
Part 1

UP COUNTER AND TESTBENCH

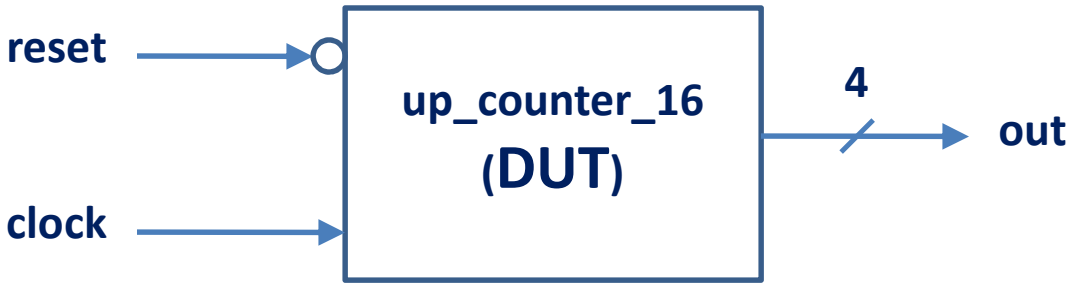
4-bit Up Counter



4-bit Up Counter (2)

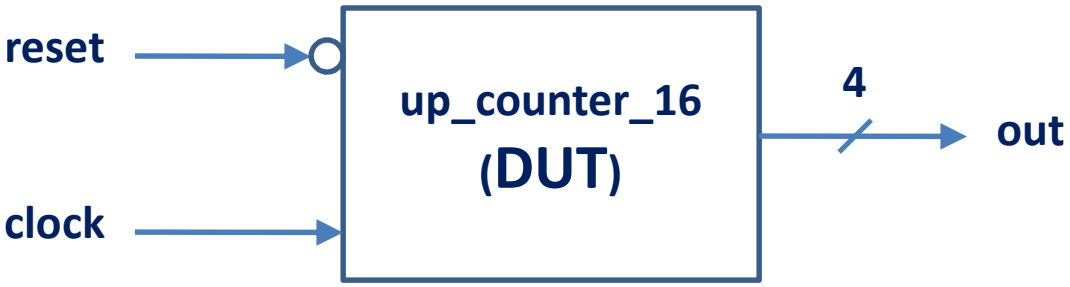


4-bit Up Counter (3)




```
1   module up_counter_16    (
2                            out,   // Output of the counter
3                            clock, // clock Input
4                            reset  // reset Input
5                            );
6
7   input clock, reset;
8   output [3:0] out;
9
10  reg [3:0] out; // internal variable
11
12  always @(posedge clock)
13      if (! reset) out <= 4'b0 ;
14      else         out <= out + 1;
15
16  endmodule
```

4-bit Up Counter (3)




```
up_counter_16 dut (
                   .clock (   ),
                   .reset (    ),
                   .out (  )
                  );
```

```
`timescale 1 ns/10 ps

module up_counter_16_tb;

reg clk;
reg rstn;
wire [3:0] out;

up_counter_16 dut (
                .clock (   ),
                .reset (    ),
                .out (  )
                );

always #5 clk = ~clk;

initial
    begin
        // 1. Initialize testbench variables to 0
        clk <= 0;
        rstn <= 0;
        // 2. Drive rest of the stimulus
        #20 rstn <= 1;
        #80 rstn <= 0;
        #50 rstn <= 1;
        // 3. Finish the stimulus after 200ns
        #20 $finish;
    end
endmodule
```

```
`timescale 1 ns/10 ps

module up_counter_16_tb;

reg clk;
reg rstn;
wire [3:0] out;

// Instantiate counter design
up_counter_16 dut (
                .clock (   ),
                .reset (    ),
                .out (  )
                );


always #5 clk = ~clk;

initial
    begin
        // 1. Initialize testbench variables to 0
        clk <= 0;
        rstn <= 0;
        // 2. Drive rest of the stimulus
        #20 rstn <= 1;
        #80 rstn <= 0;
        #50 rstn <= 1;
        // 3. Finish the stimulus after 200ns
        #20 $finish;
    end
endmodule
```

```
`timescale 1 ns/10 ps

module up_counter_16_tb;

reg clk;
reg rstn;
wire [3:0] out;

// Instantiate counter design
up_counter_16 dut (
                .clock (clk),
                .reset (rstn),
                .out (out)
                );


always #5 clk = ~clk;

initial
    begin
        // 1. Initialize testbench variables to 0
        clk <= 0;
        rstn <= 0;
        // 2. Drive rest of the stimulus
        #20 rstn <= 1;
        #80 rstn <= 0;
        #50 rstn <= 1;
        // 3. Finish the stimulus after 200ns
        #20 $finish;
    end
endmodule
```

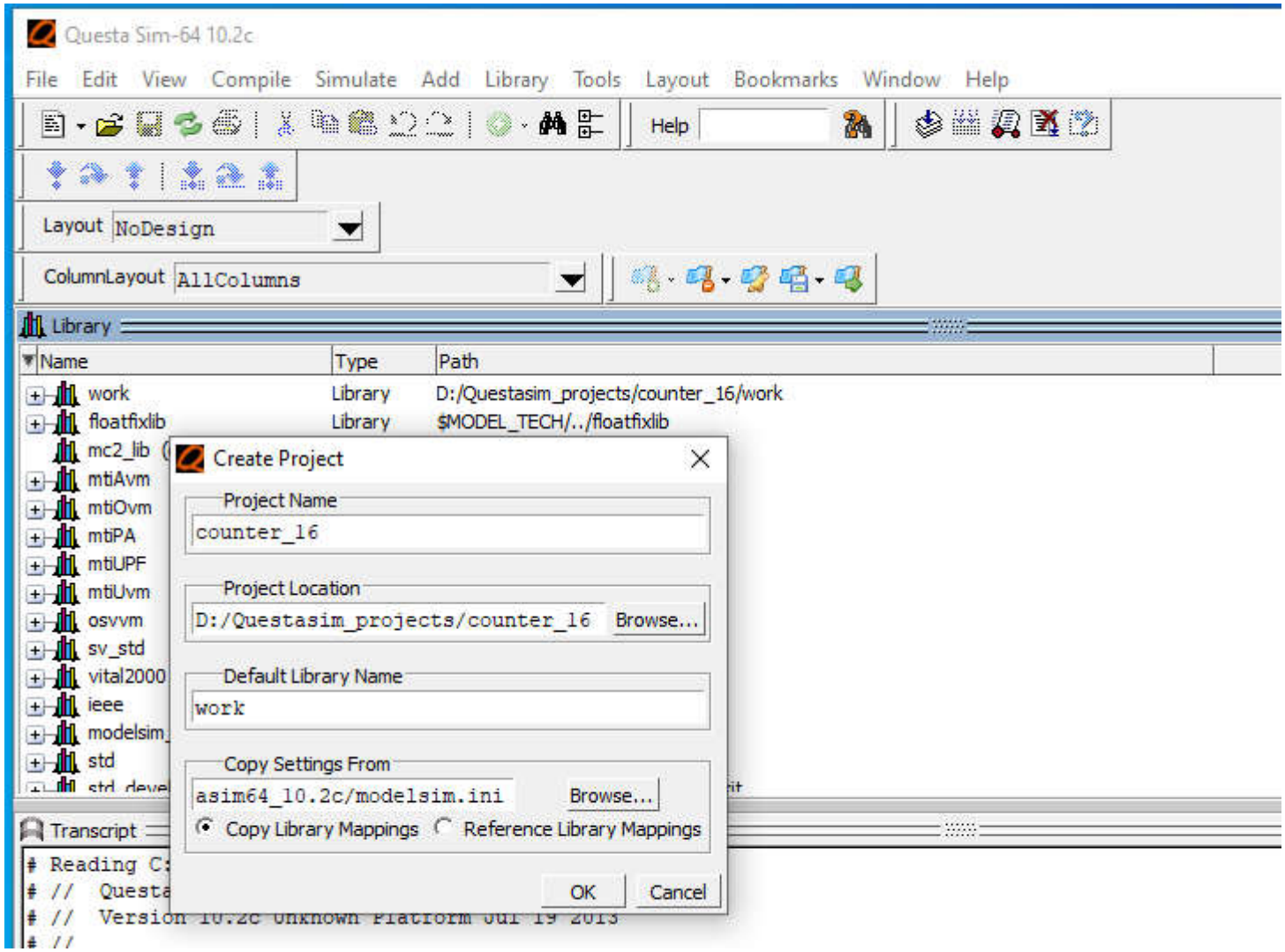
Part 2

ADD TO WAVE (HOMEWORK)

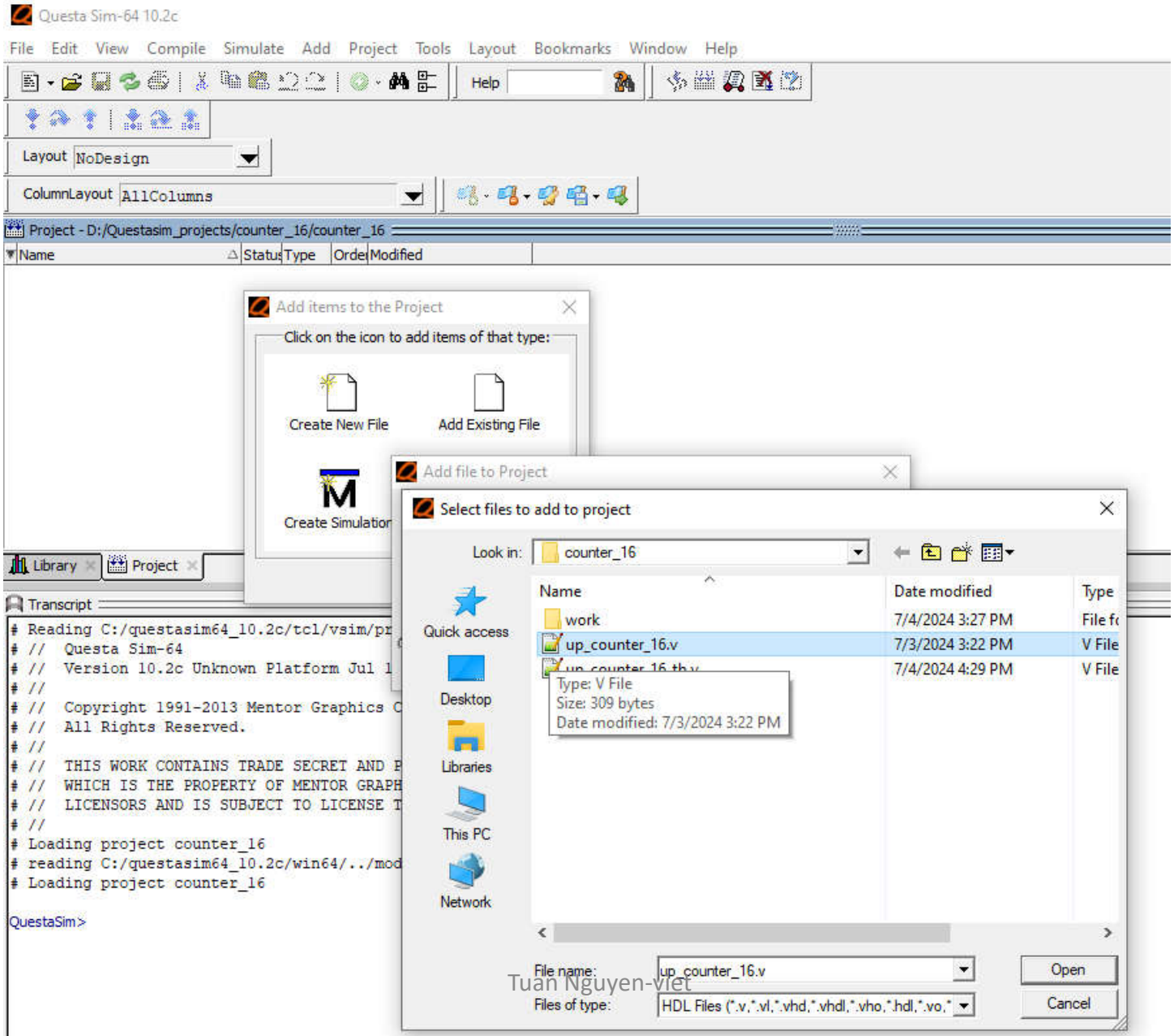
Part 3

ADD TO LIST

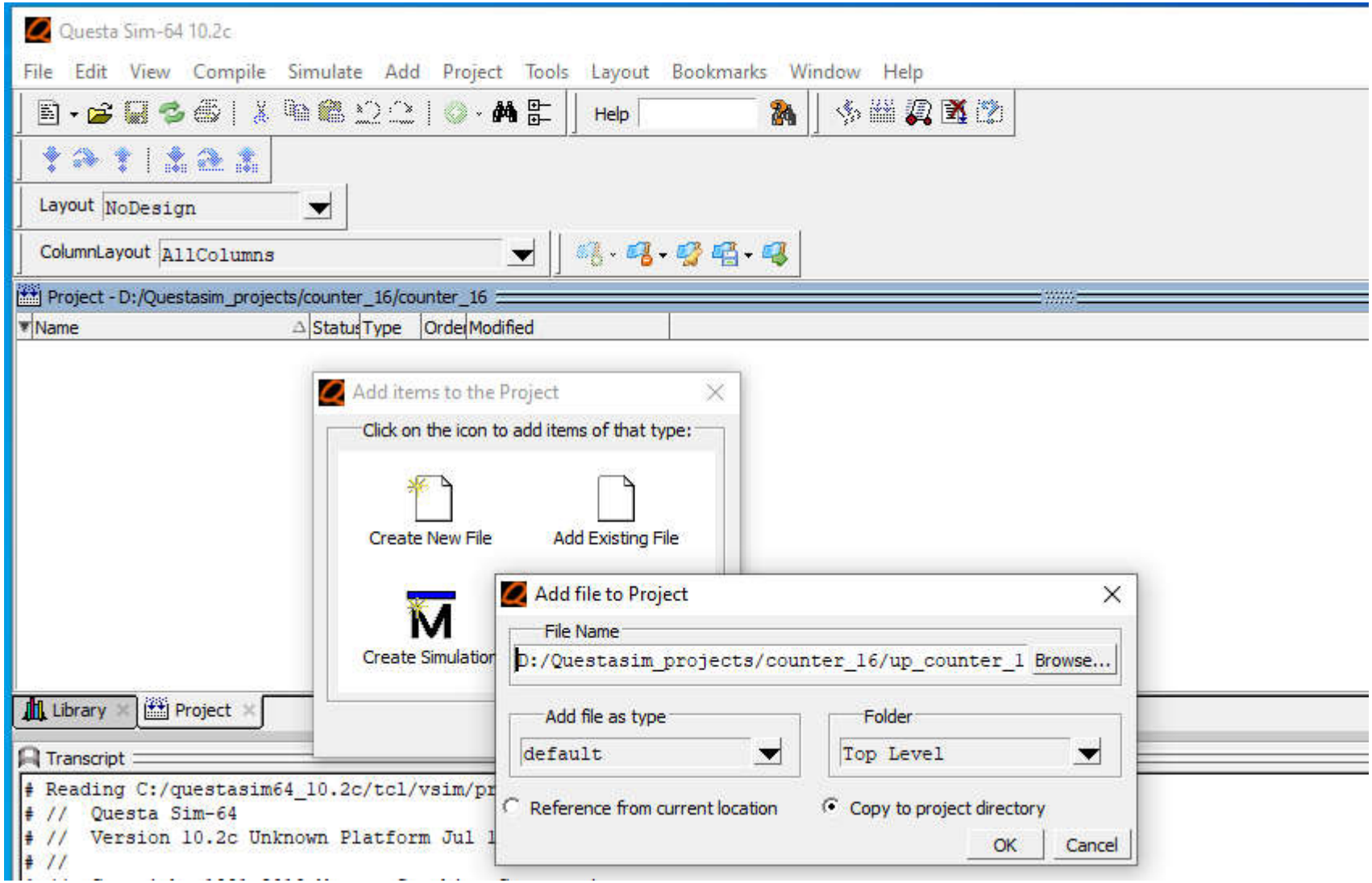
Project 1.Directory / 2.Name / 3.Location: counter_16



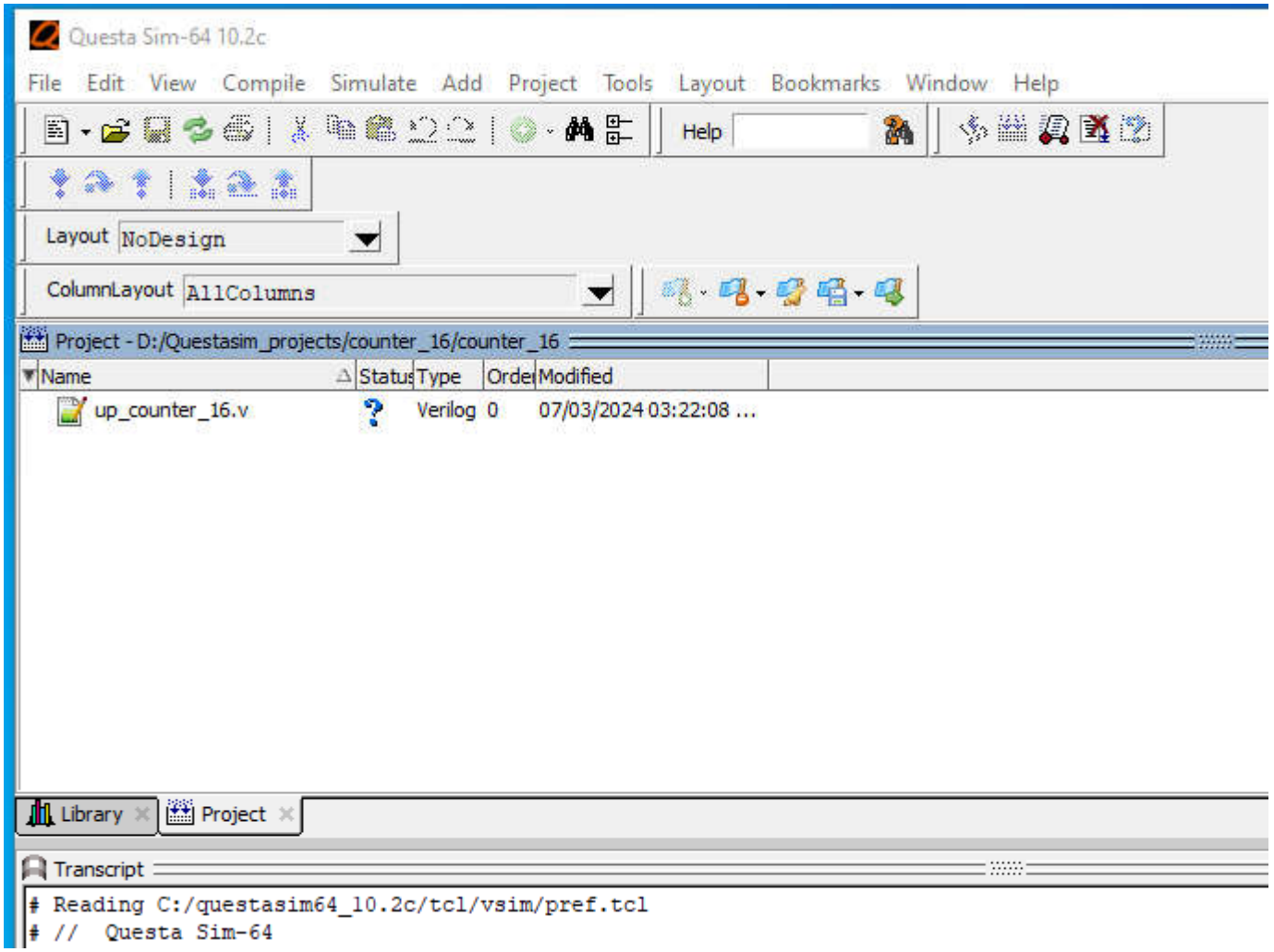
Add Design file only: up_counter_16.v



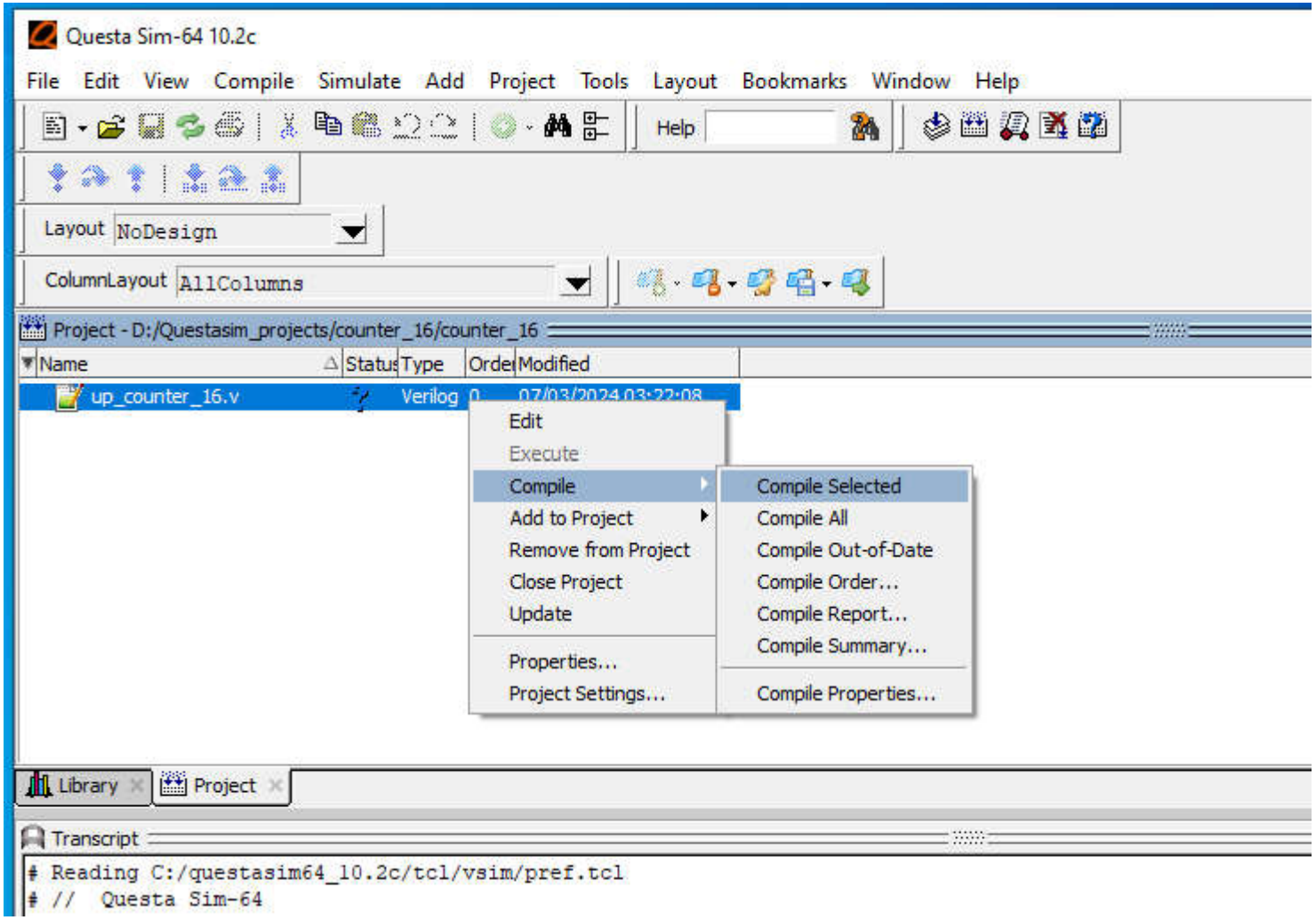
Add Design file only: up_counter_16.v (2)



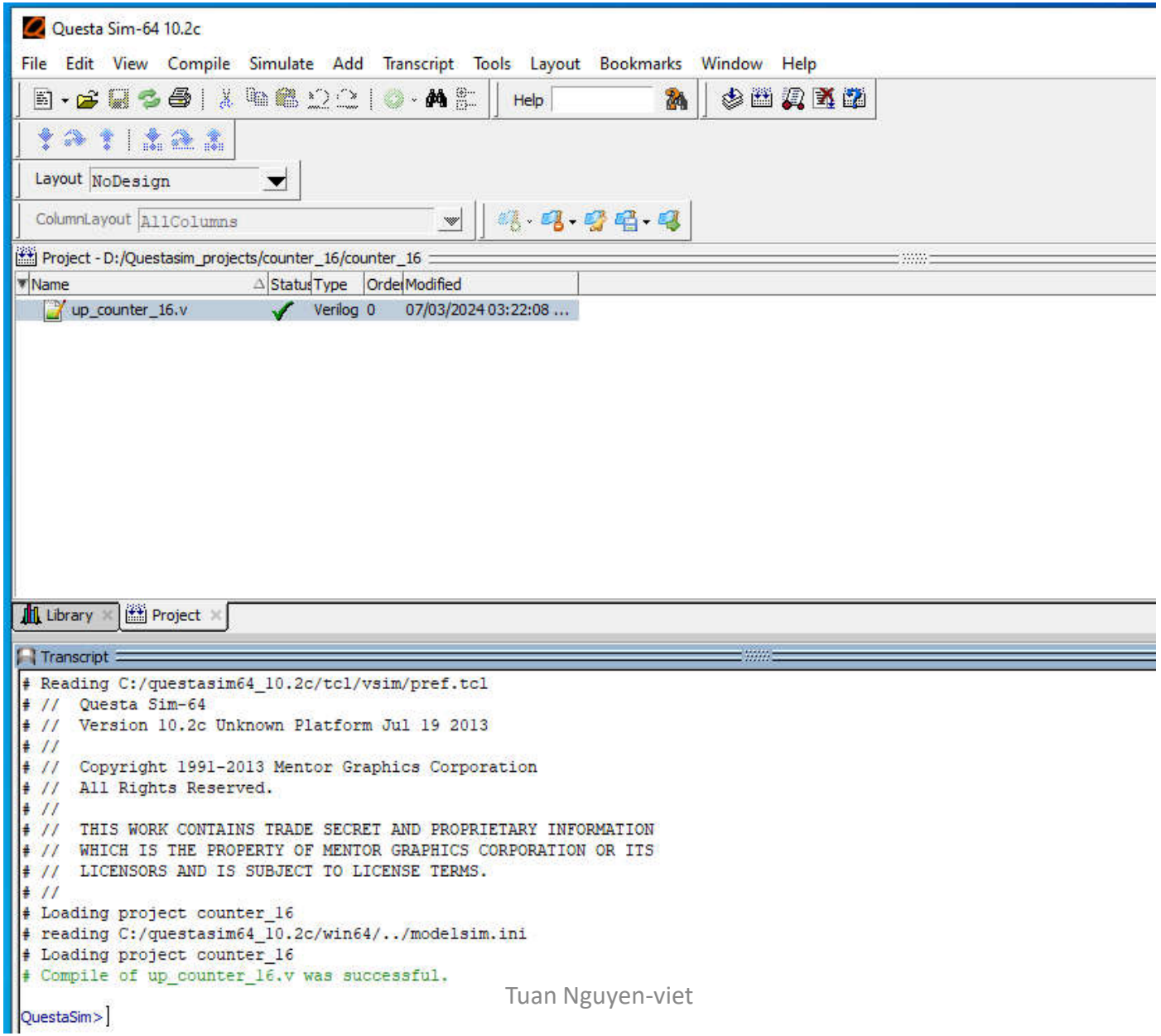
Add Design file only: up_counter_16.v (3)



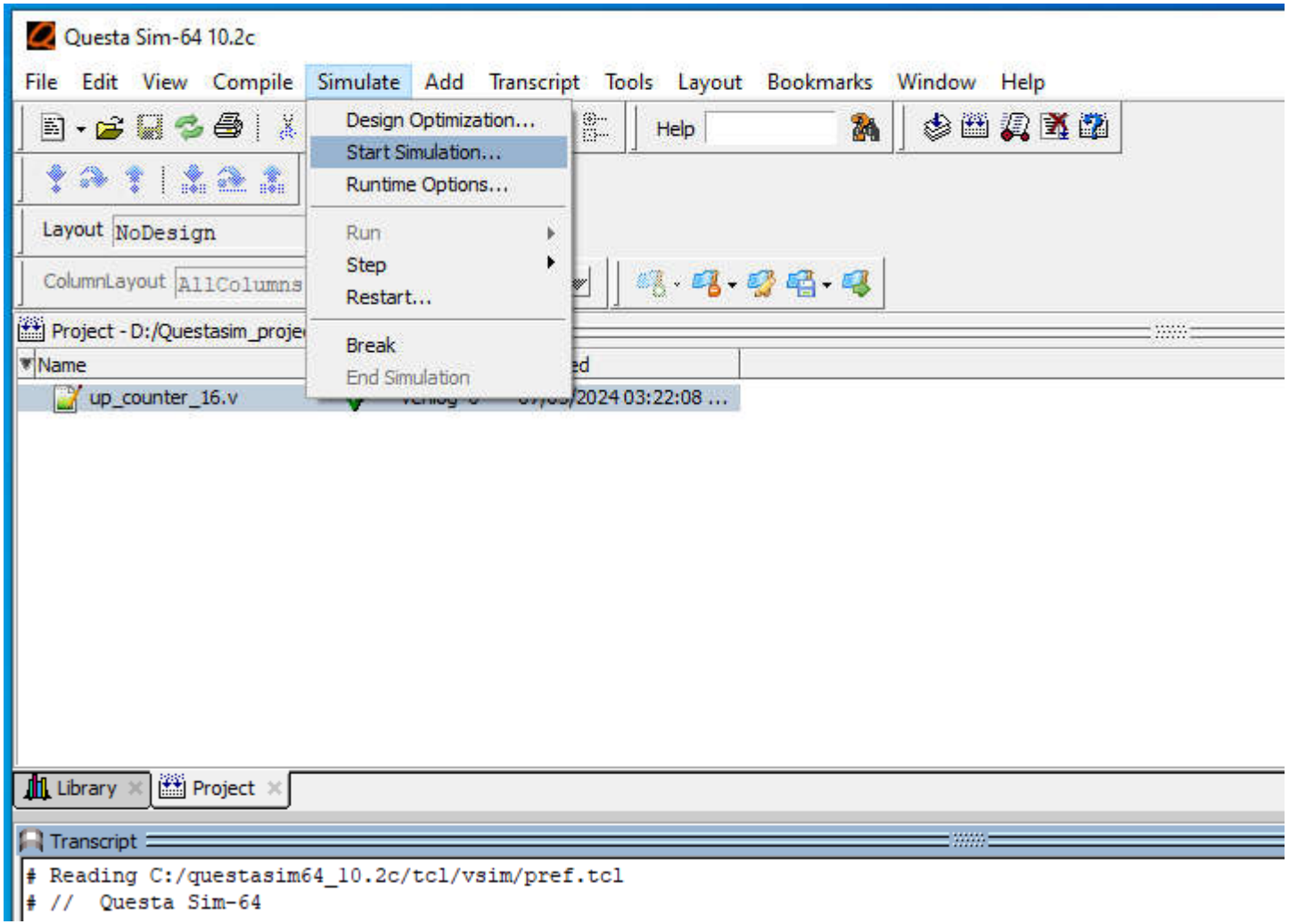
Compile Design file: up_counter_16.v



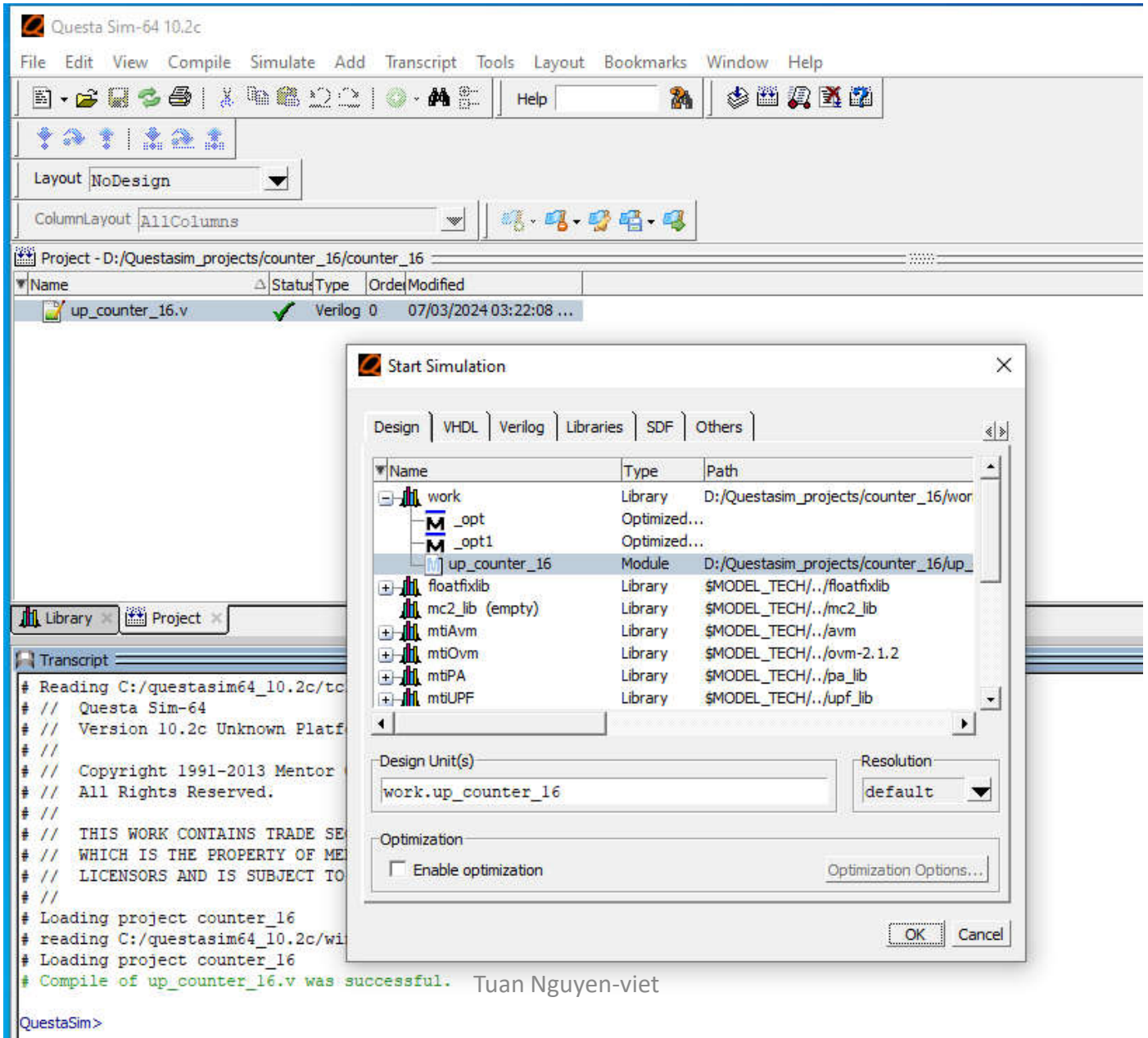
Compile Design file: up_counter_16.v (2)



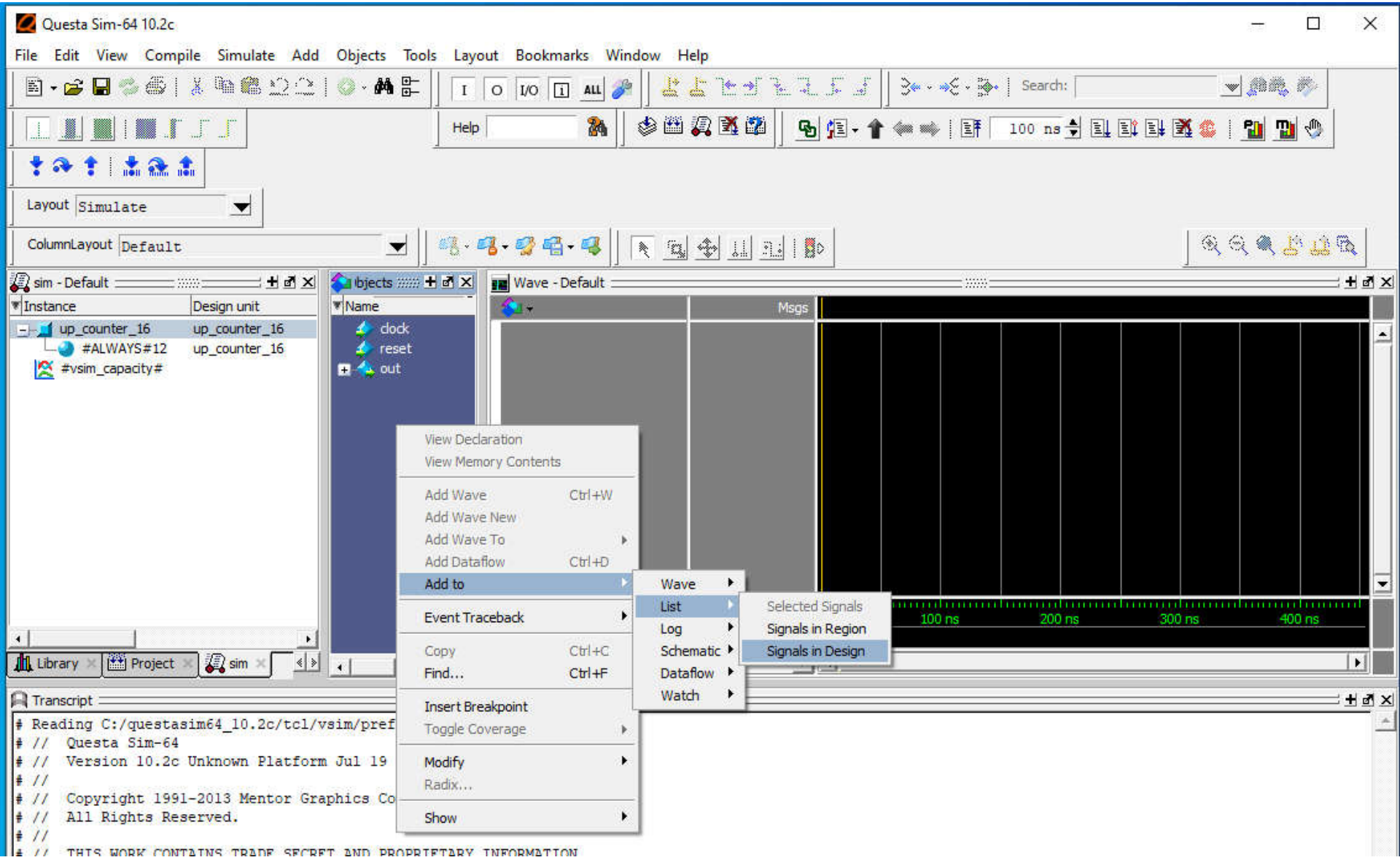
Start Simulation



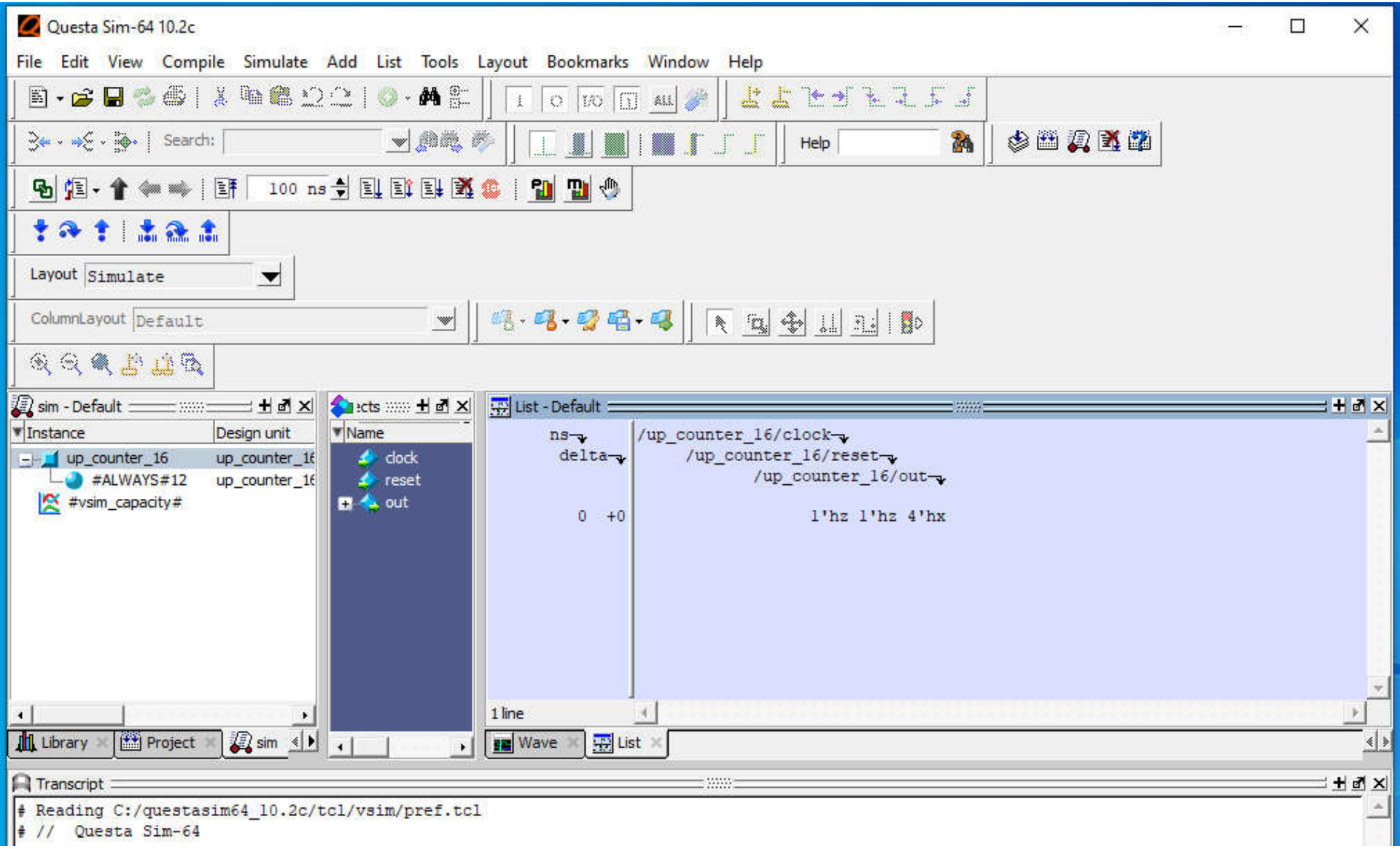
Start Simulation (2)



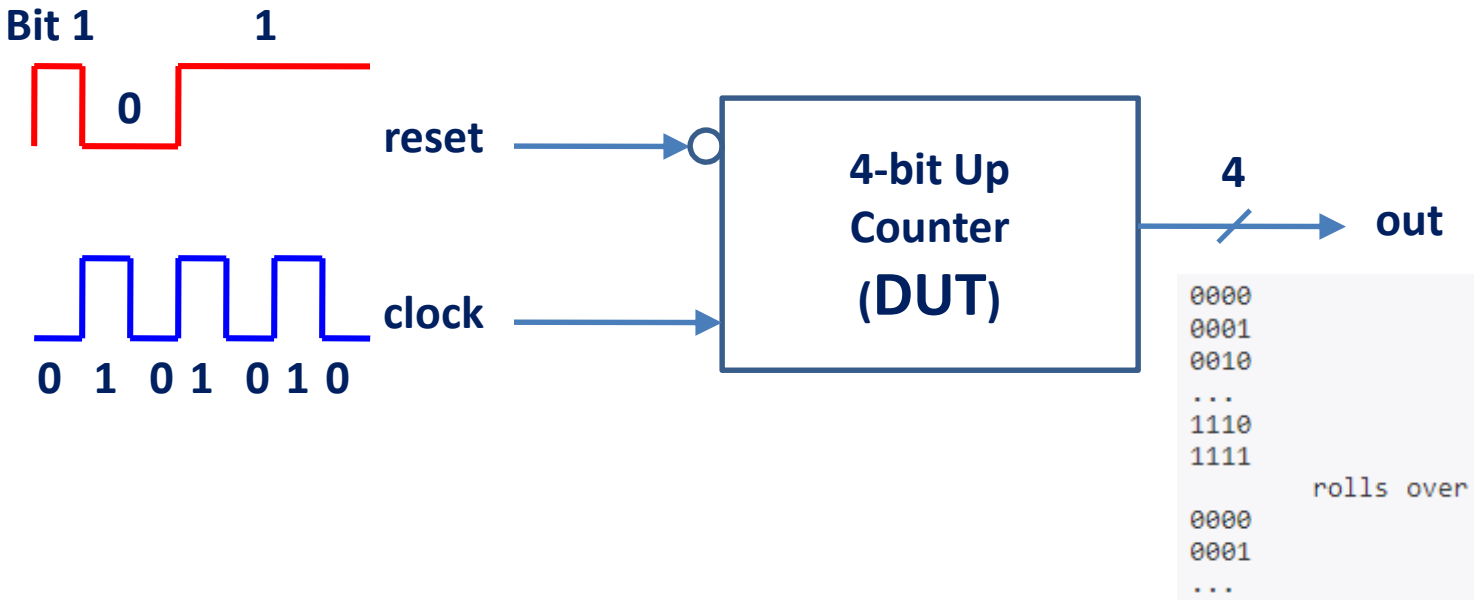
Add to List (different from 'Add to Wave')



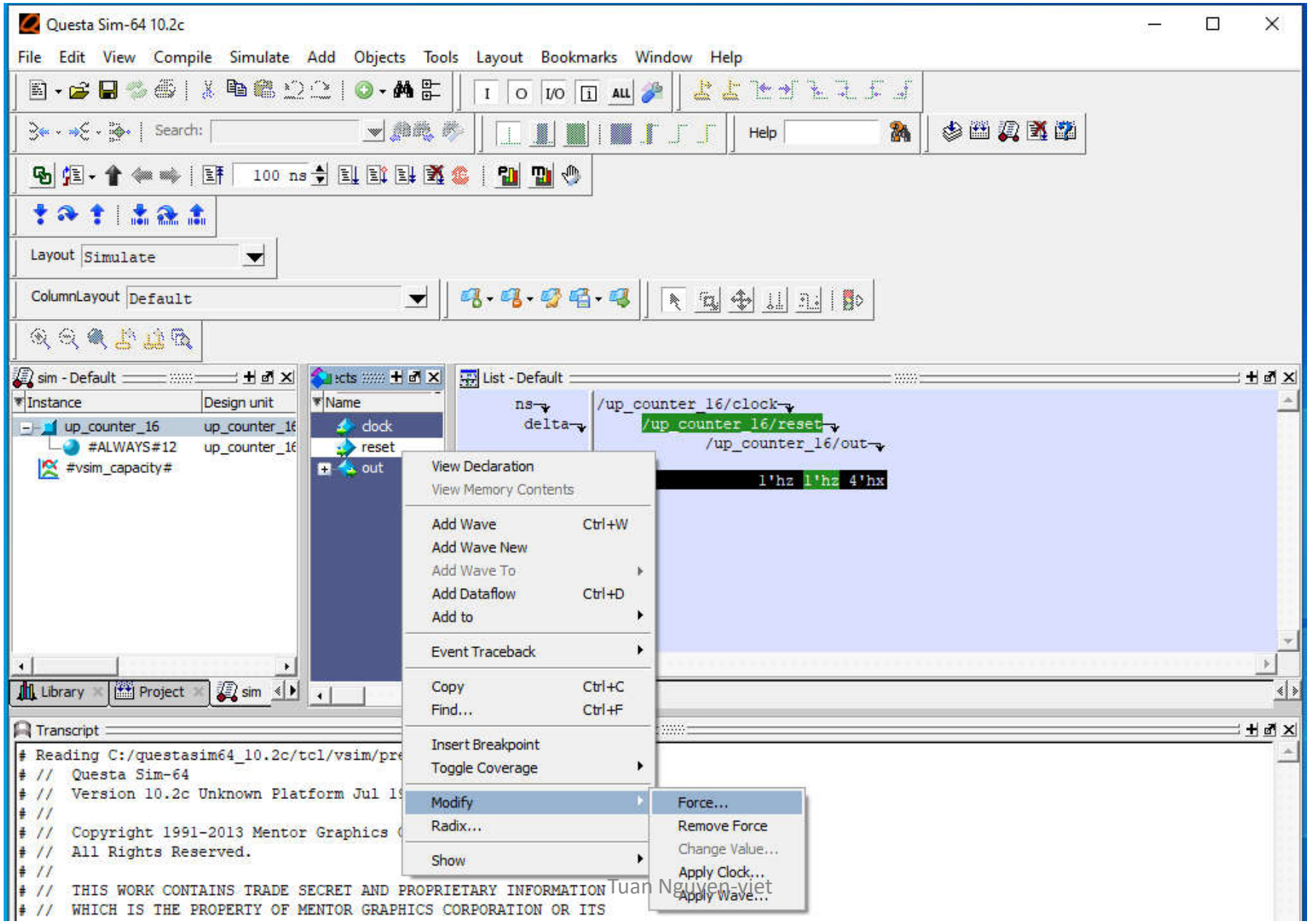
Add to List (2)


Questa Sim-64 10.2c
File Edit View Compile Simulate Add List Tools Layout Bookmarks Window Help
Search:
Help
100 ns
Layout Simulate
ColumnLayout Default
sim - Default
Instance
Design unit
up_counter_16
up_counter_16
#ALWAYS#12
up_counter_16
#vsim_capacity#
Name
clock
reset
out
List - Default
ns
delta
/up_counter_16/clock
/up_counter_16/reset
/up_counter_16/out
0 +0
1'hz 1'hz 4'hx
1 line
Library
Project
sim
Wave
List
Transcript
Reading C:/questasim64_10.2c/tcl/vsim/pref.tcl
// Questa Sim-64

Force Reset and apply Clock

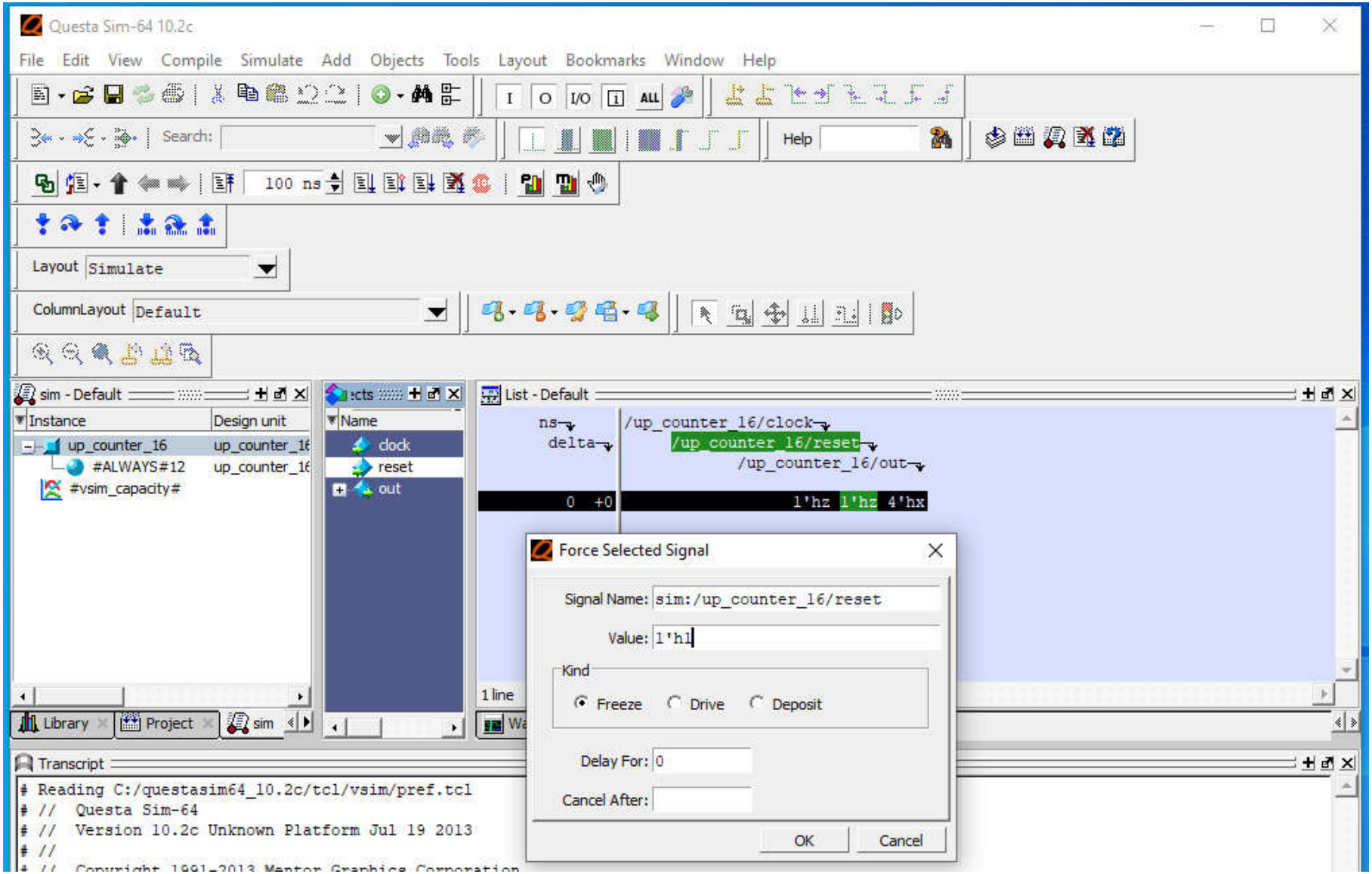


Add to List: Force Reset signal to ‘1’

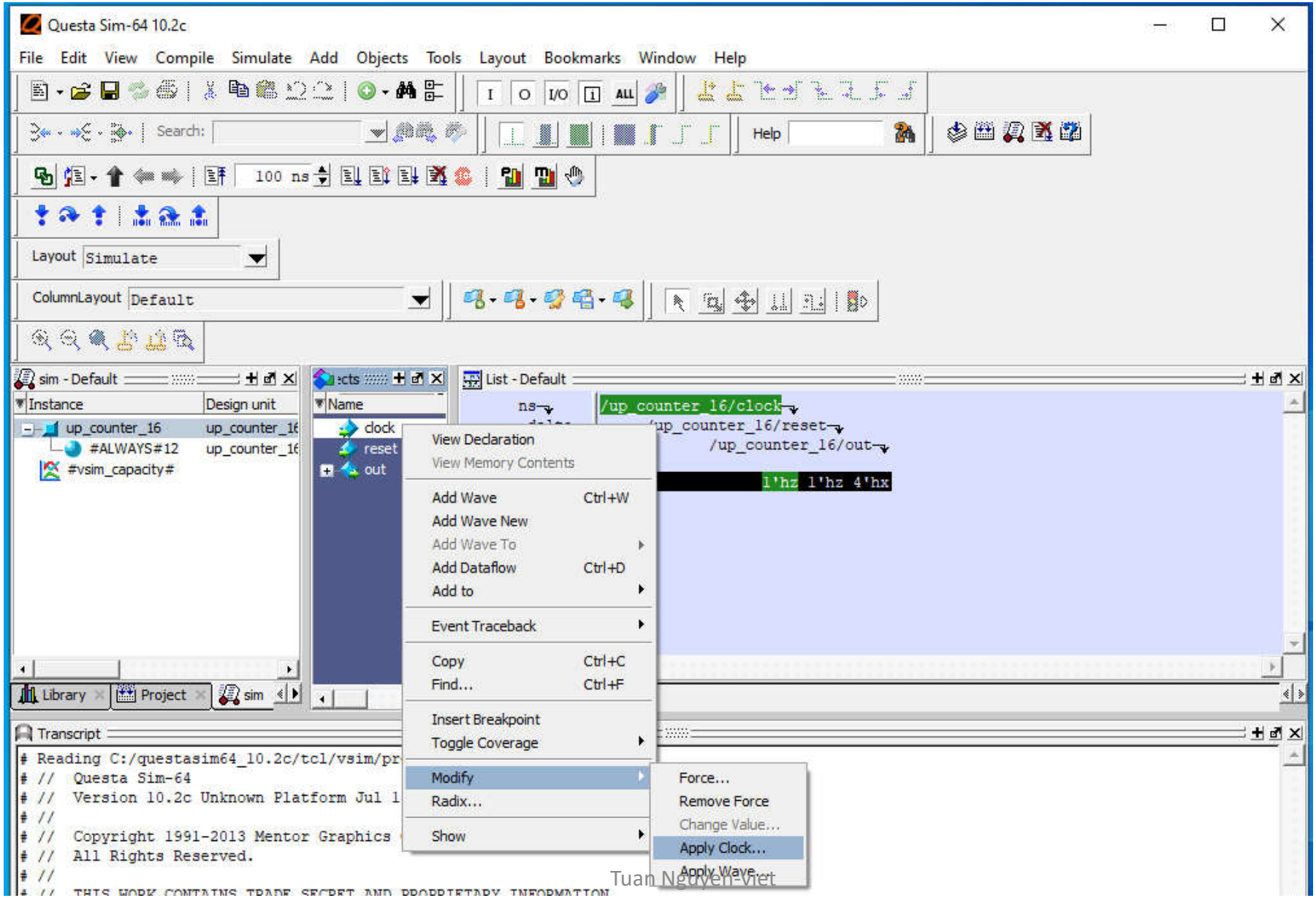


Tuan Nguyen-viet

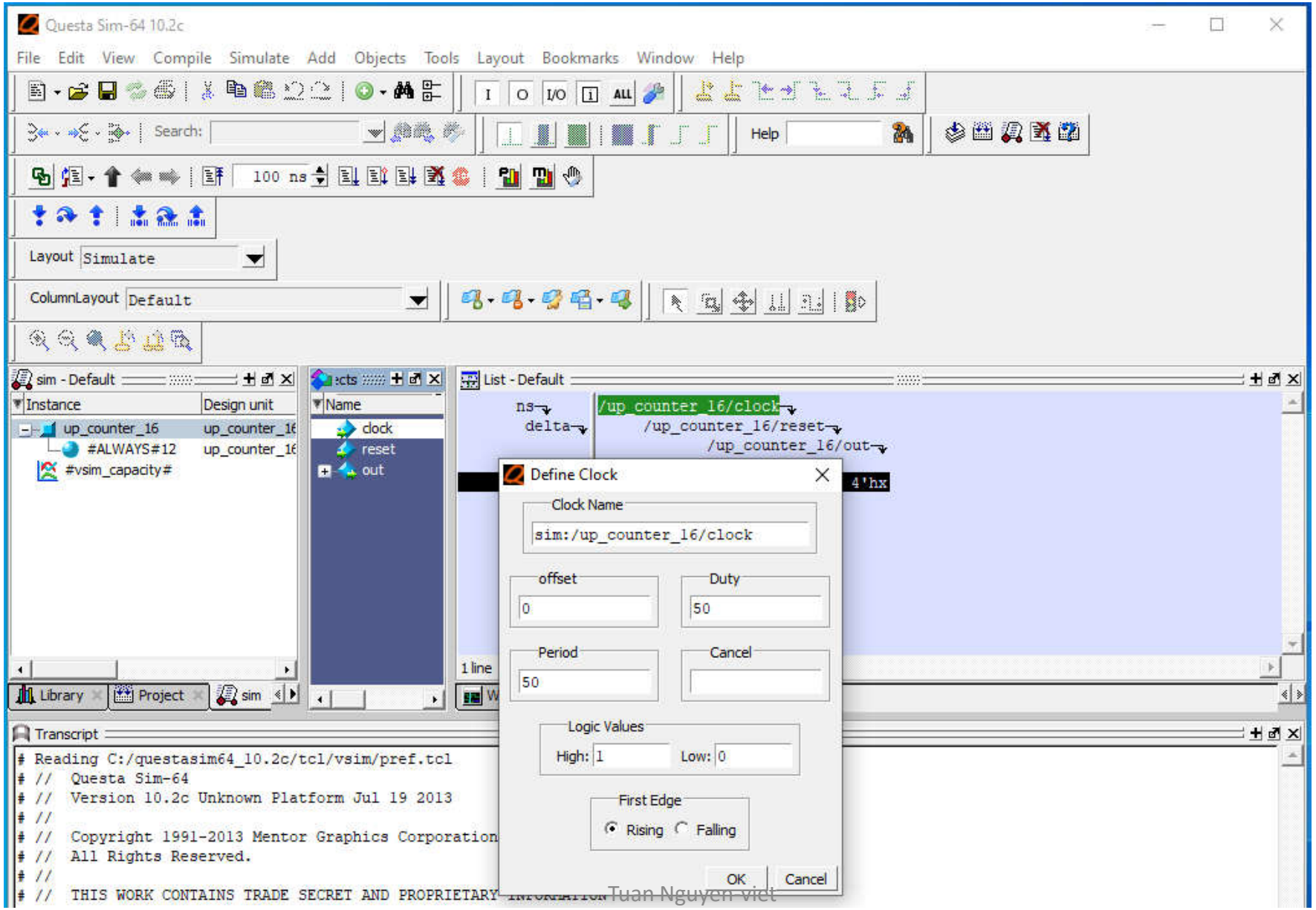
Add to List: Force Reset signal to ‘1’ (2)



Add to List: Apply Clock signal



Add to List: Apply Clock signal (2)

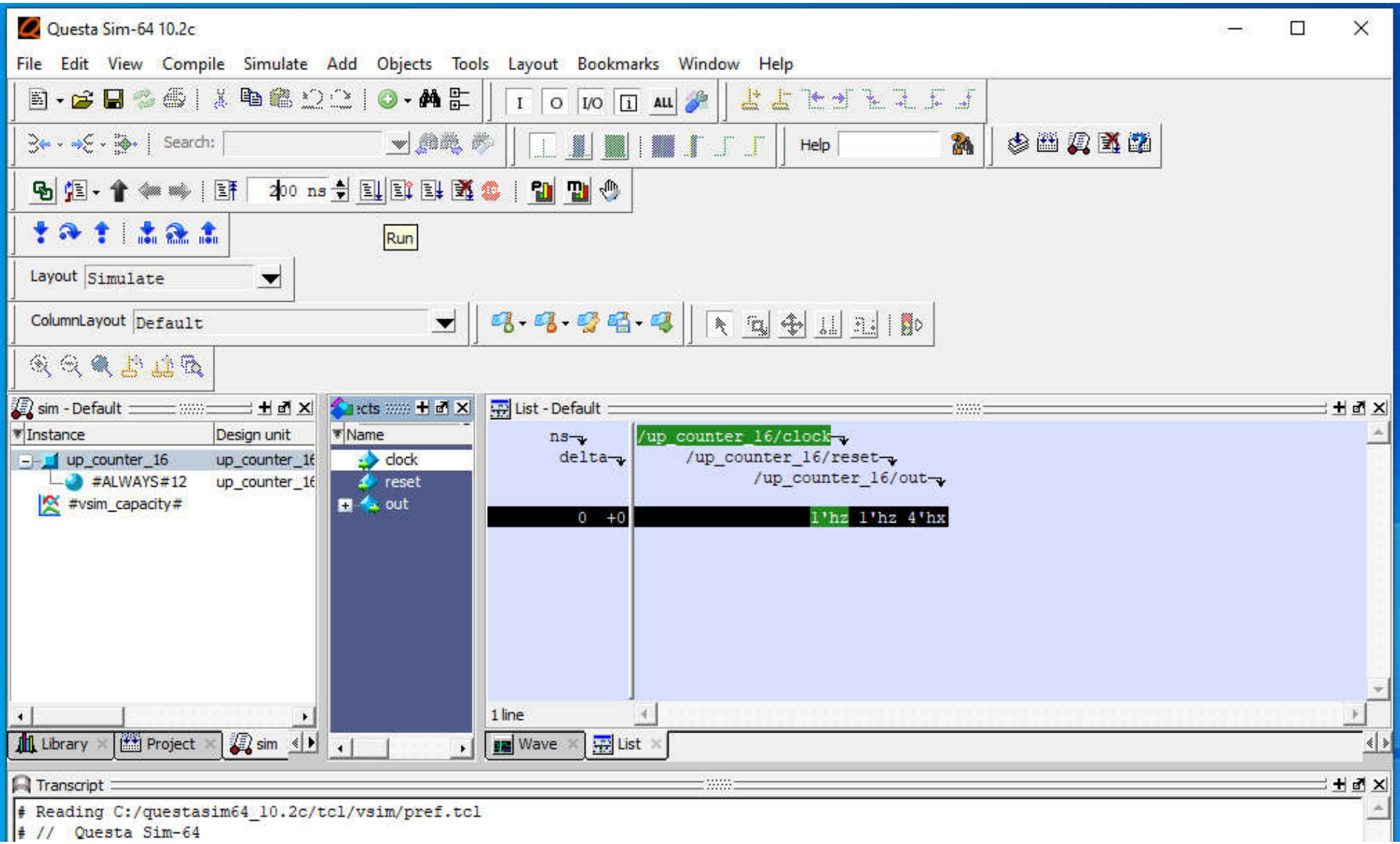


Tuan Nguyen viet

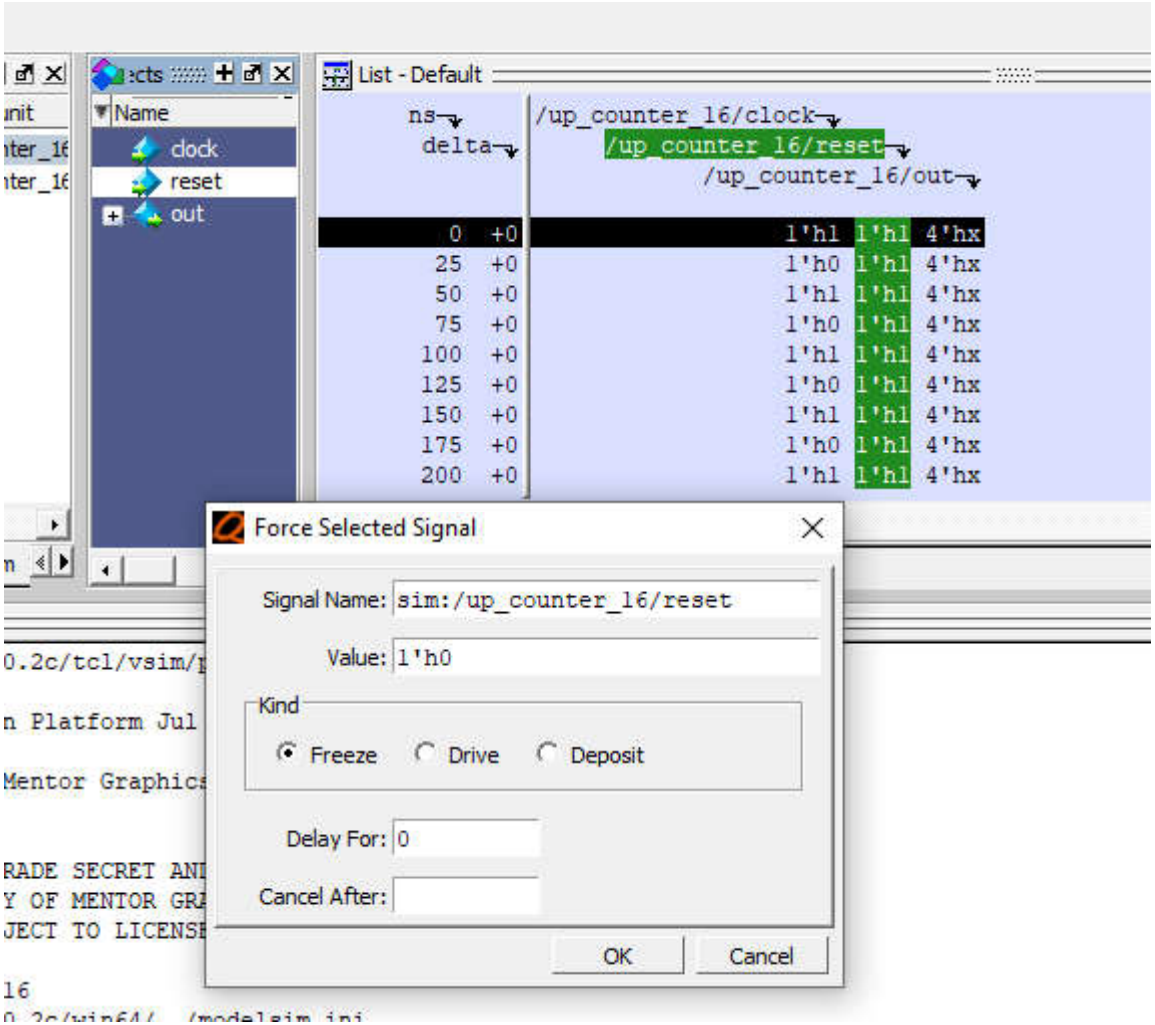
```
# //
# Loading project counter_16
# reading C:/questasim64_10.2c/win64/../modelsim.ini
# Loading project counter_16
# Compile of up_counter_16.v was successful.
QuestaSim> vsim -gui -novopt work.up_counter_16
# vsim -gui -novopt work.up_counter_16
# Refreshing D:/Questasim_projects/counter_16/work.up_counter_16
# Loading work.up_counter_16
add list -r /*
force -freeze sim:/up_counter_16/reset 1'h1 0
force -freeze sim:/up_counter_16/clock 1 0, 0 {25 ns} -r 50

VSIM 5>
```

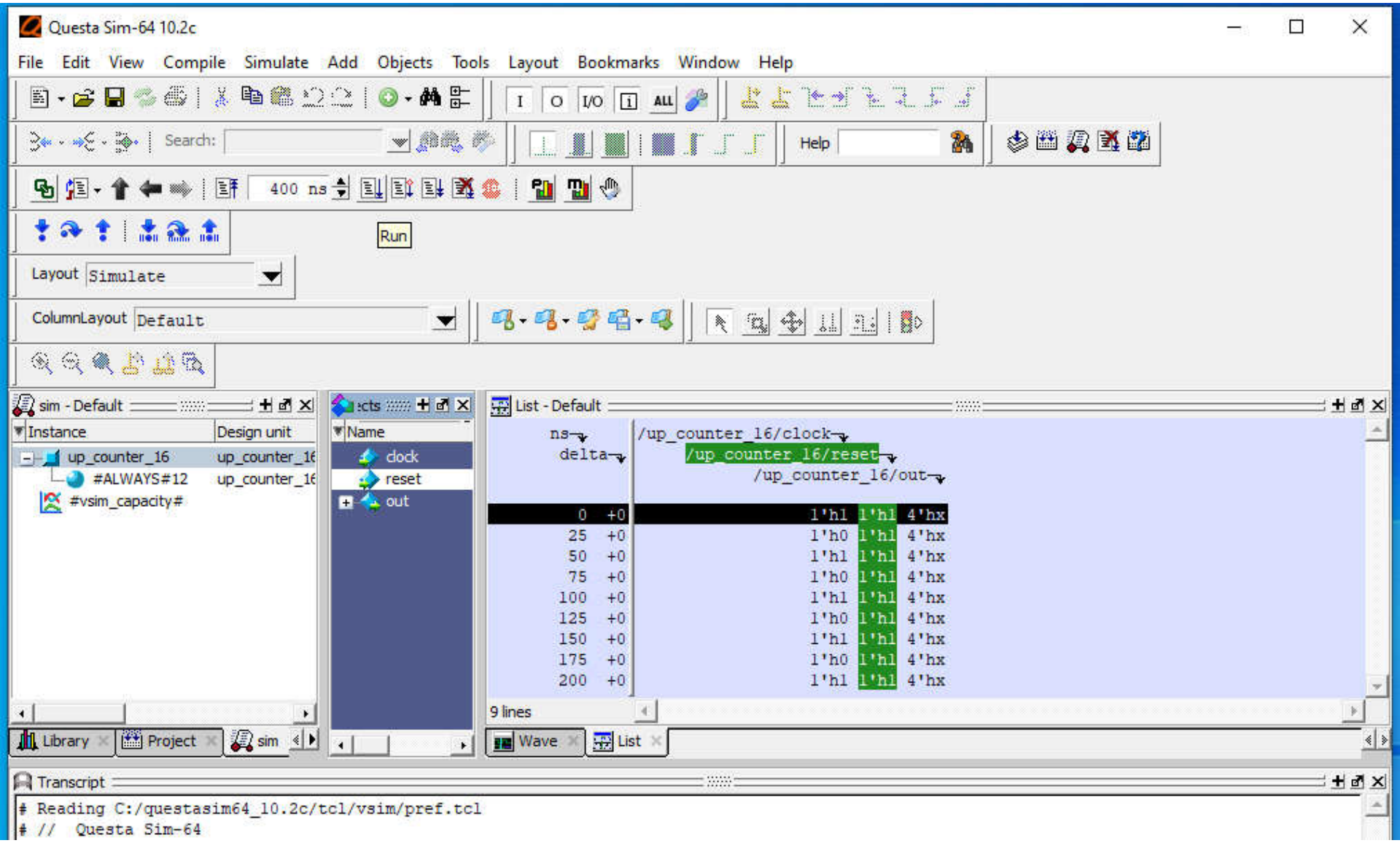
Run Simulation



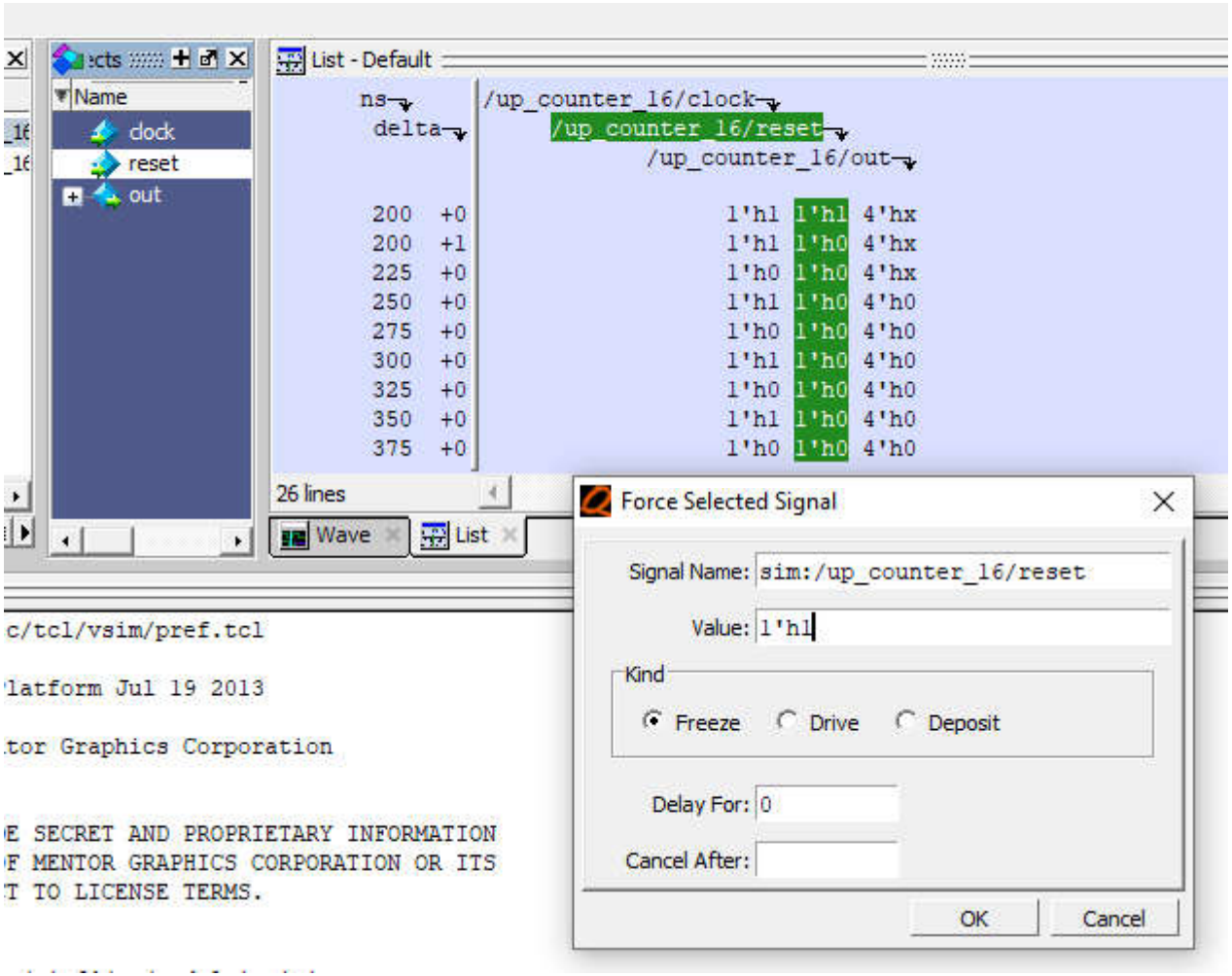
Result in the First Time and Force Reset to ‘0’



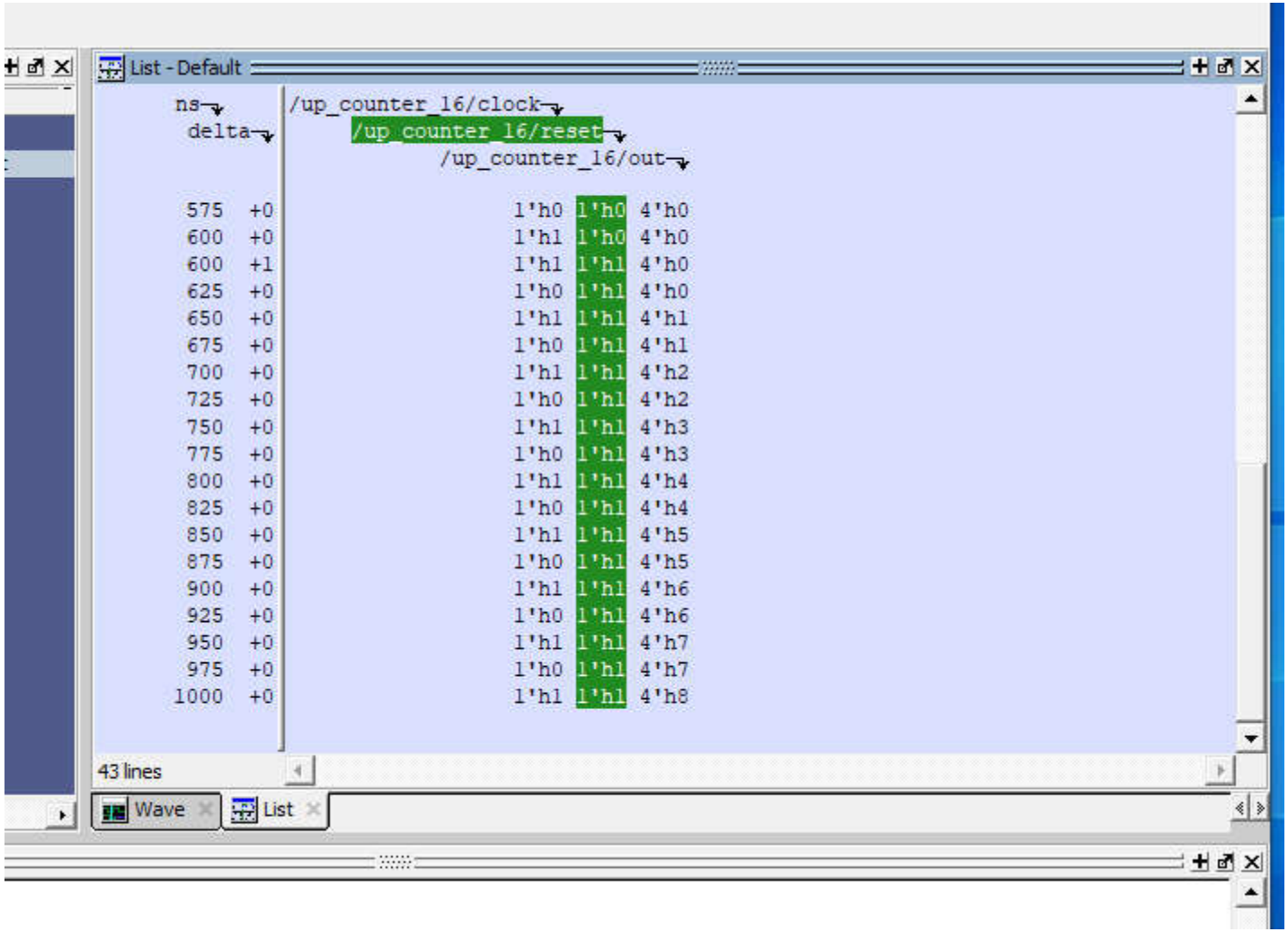
Run Sim again with 400 ns



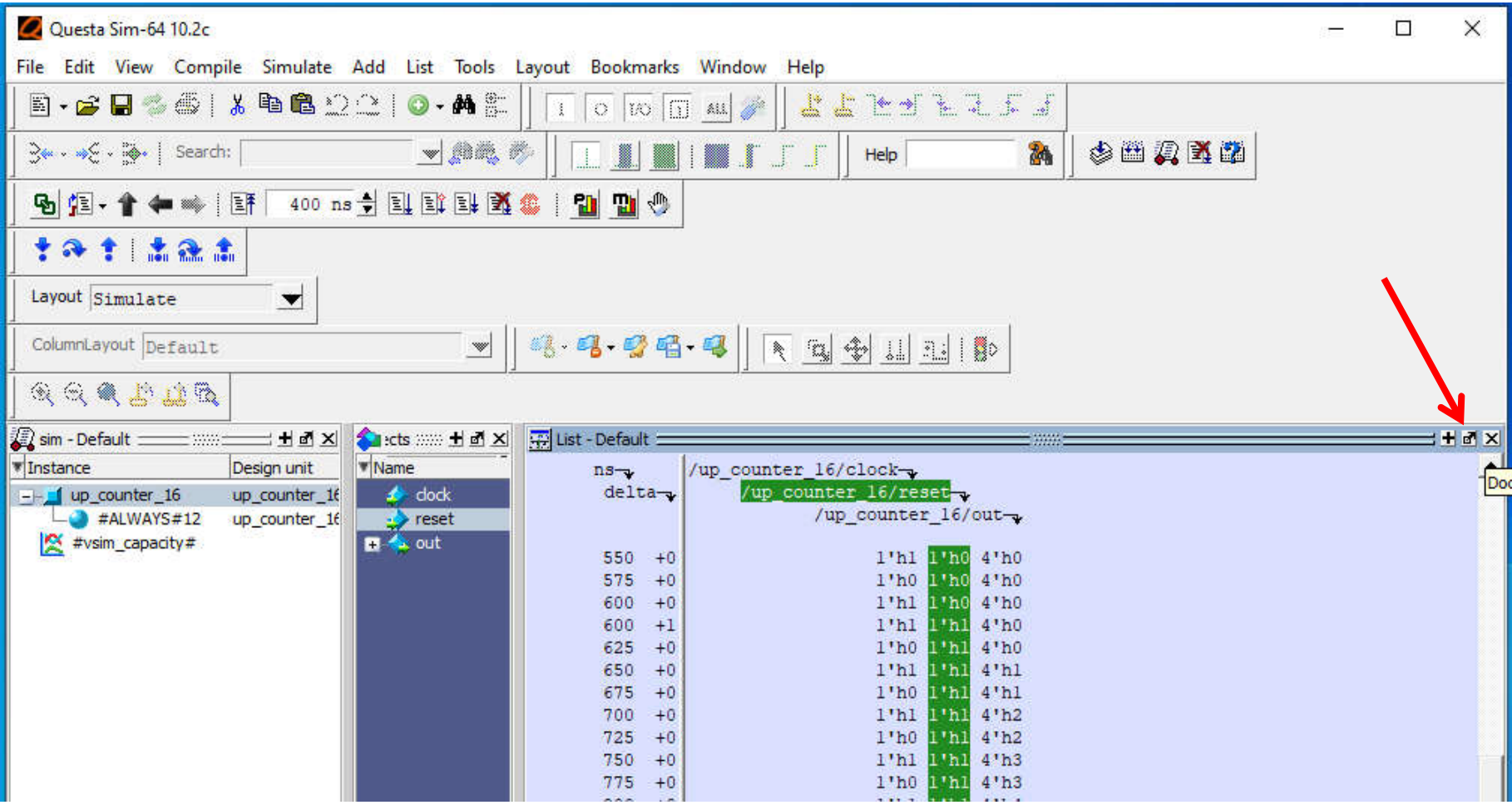
Result in the Second Time and Force Reset to ‘1’



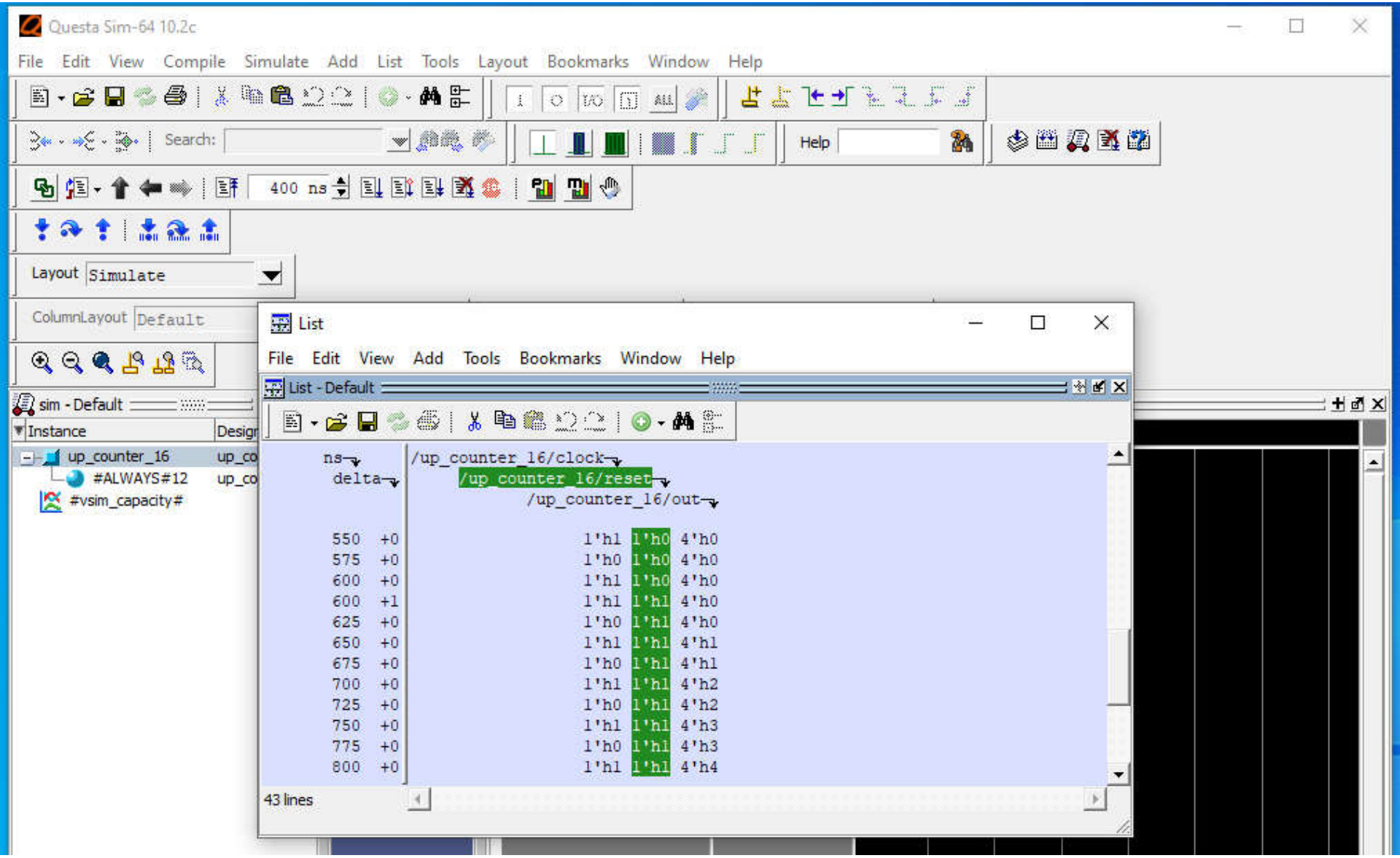
Run Sim once more with 400 ns



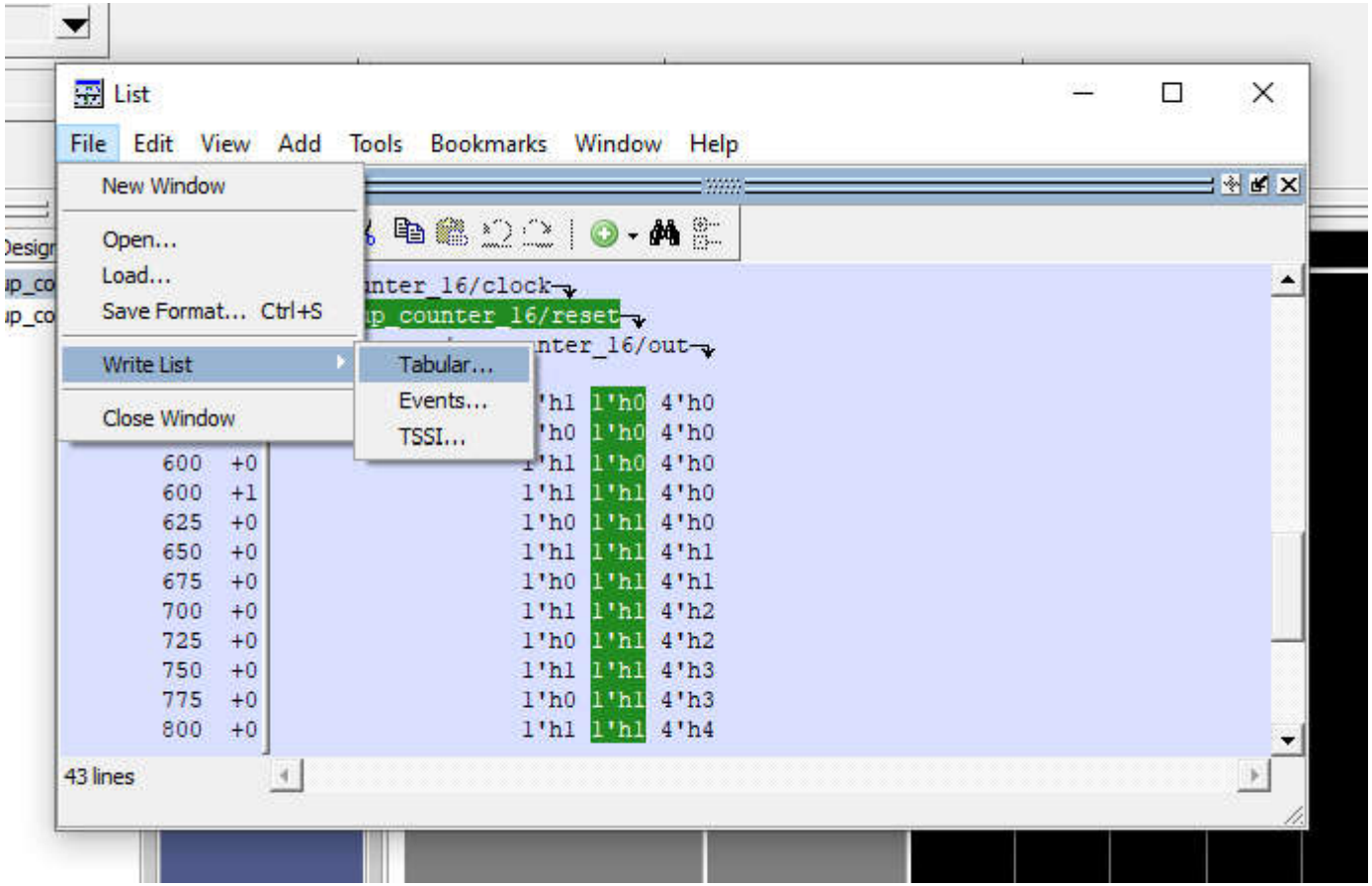
Undocking the List window



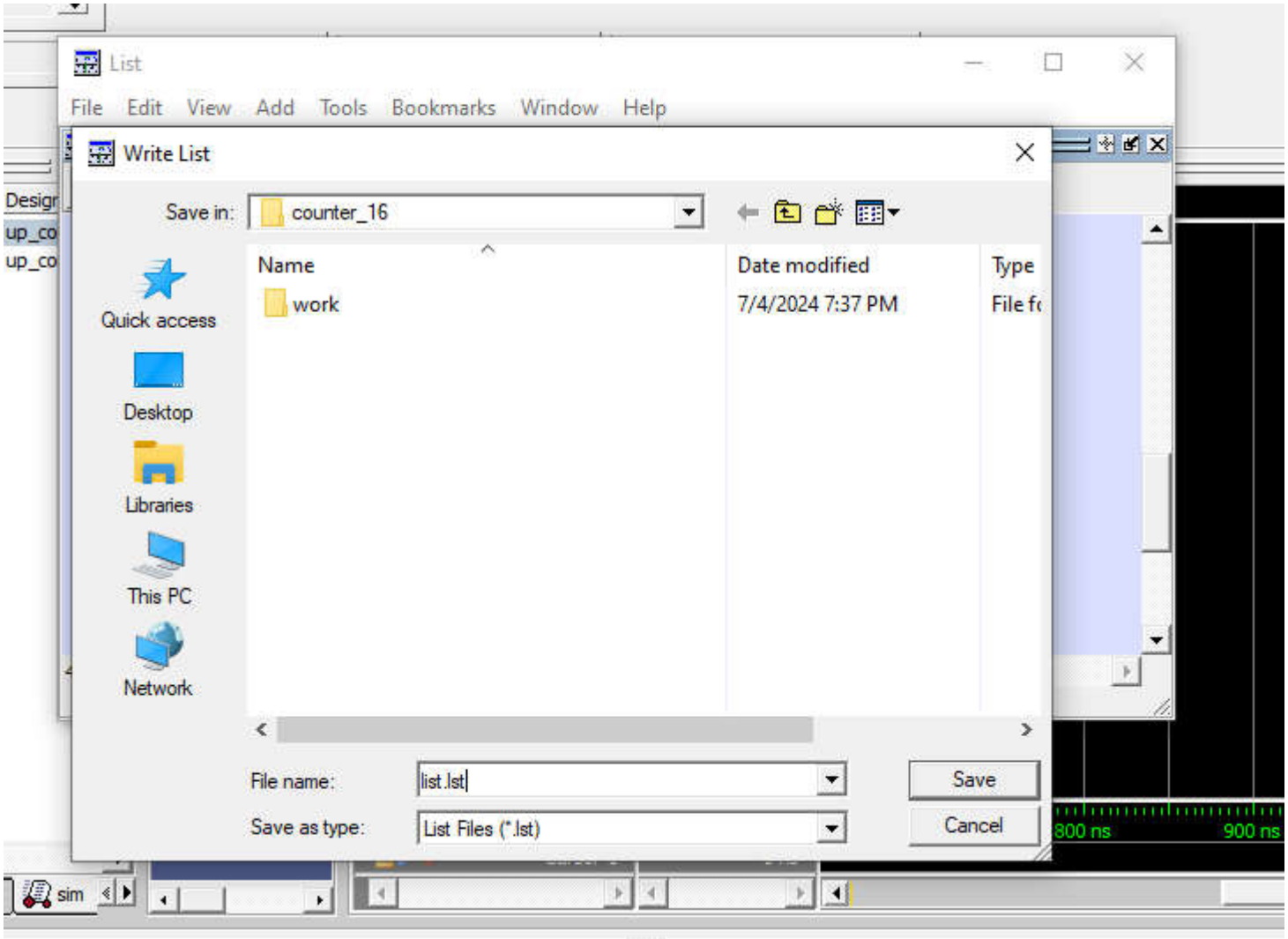
List window


Questa Sim-64 10.2c
File Edit View Compile Simulate Add List Tools Layout Bookmarks Window Help
Search:
Help
400 ns
Layout Simulate
ColumnLayout Default
sim - Default
Instance
up_counter_16
#ALWAYS#12
#vsim_capacity#
List
File Edit View Add Tools Bookmarks Window Help
List - Default
ns
delta
/up_counter_16/clock
/up_counter_16/reset
/up_counter_16/out
550 +0 1'h1 1'h0 4'h0
575 +0 1'h0 1'h0 4'h0
600 +0 1'h1 1'h0 4'h0
600 +1 1'h1 1'h1 4'h0
625 +0 1'h0 1'h1 4'h0
650 +0 1'h1 1'h1 4'h1
675 +0 1'h0 1'h1 4'h1
700 +0 1'h1 1'h1 4'h2
725 +0 1'h0 1'h1 4'h2
750 +0 1'h1 1'h1 4'h3
775 +0 1'h0 1'h1 4'h3
800 +0 1'h1 1'h1 4'h4
43 lines

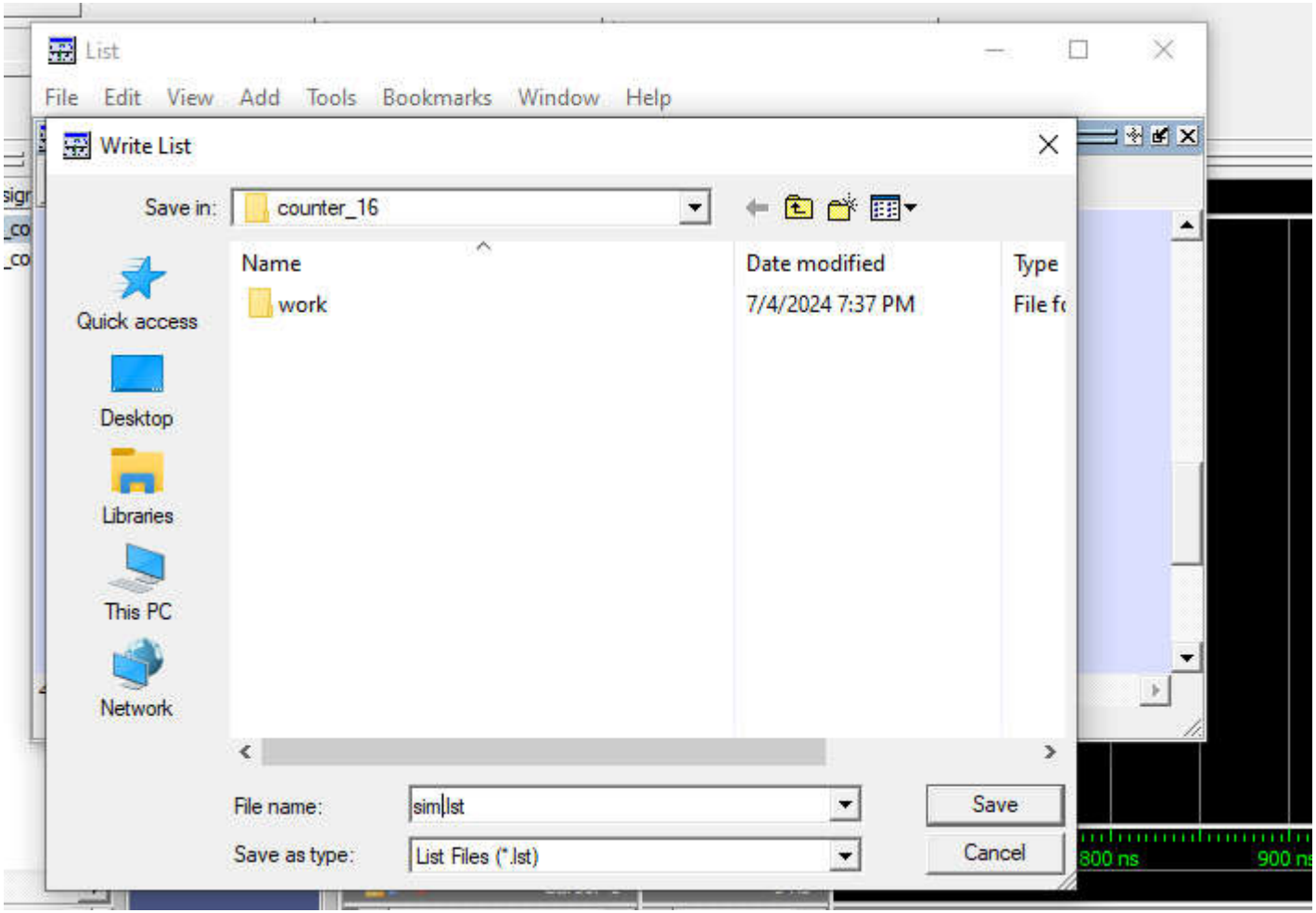
Save Sim Data to a .lst file



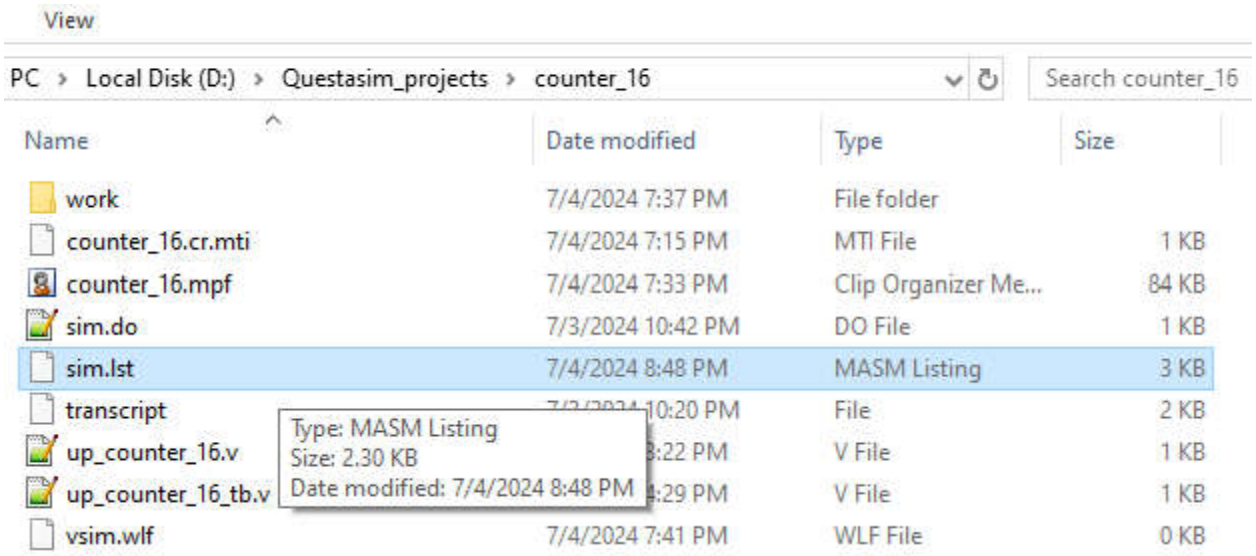
Save Sim Data to a .lst file (2)



Save Sim Data to sim.lst file



sim.lst exists in directory ‘counter_16’



Sim Data in sim.lst

sim.lst - Notepad

File Edit Format View Help

```
          ns       /up_counter_16/clock
           delta        /up_counter_16/reset
                                /up_counter_16/out
           0  +0                    1'h1 1'h1 4'hx
          25  +0                    1'h0 1'h1 4'hx
          50  +0                    1'h1 1'h1 4'hx
          75  +0                    1'h0 1'h1 4'hx
         100  +0                    1'h1 1'h1 4'hx
         125  +0                    1'h0 1'h1 4'hx
         150  +0                    1'h1 1'h1 4'hx
         175  +0                    1'h0 1'h1 4'hx
         200  +0                    1'h1 1'h1 4'hx
         200  +1                    1'h1 1'h0 4'hx
         225  +0                    1'h0 1'h0 4'hx
         250  +0                    1'h1 1'h0 4'h0
         275  +0                    1'h0 1'h0 4'h0
         300  +0                    1'h1 1'h0 4'h0
         325  +0                    1'h0 1'h0 4'h0
         350  +0                    1'h1 1'h0 4'h0
         375  +0                    1'h0 1'h0 4'h0
         400  +0                    1'h1 1'h0 4'h0
         425  +0                    1'h0 1'h0 4'h0
         450  +0                    1'h1 1'h0 4'h0
         475  +0                    1'h0 1'h0 4'h0
         500  +0                    1'h1 1'h0 4'h0
         525  +0                    1'h0 1'h0 4'h0
         550  +0                    1'h1 1'h0 4'h0
         575  +0                    1'h0 1'h0 4'h0
         600  +0                    1'h1 1'h0 4'h0
         600  +1                    1'h1 1'h1 4'h0
         625  +0                    1'h0 1'h1 4'h0
         650  +0                    1'h1 1'h1 4'h1
         675  +0                    1'h0 1'h1 4'h1
         700  +0                    1'h1 1'h1 4'h2
         725  +0                    1'h0 1'h1 4'h2
         750  +0                    1'h1 1'h1 4'h3
         775  +0                    1'h0 1'h1 4'h3
         800  +0                    1'h1 1'h1 4'h4
         825  +0                    1'h0 1'h1 4'h4
         850  +0                    1'h1 1'h1 4'h5
         875  +0                    1'h0 1'h1 4'h5
         900  +0                    1'h1 1'h1 4'h6
         925  +0                    1'h0 1'h1 4'h6
         950  +0                    1'h1 1'h1 4'h7
         975  +0                    1'h0 1'h1 4'h7
```

Thank You