# Questasim Tutorial (GUI/Windows) Continued

**REF: ModelSim® Tutorial** Software Version 10.4c

Part 1

#### **UP COUNTER AND TESTBENCH**

## **4-bit Up Counter**





# 4-bit Up Counter (2)



# 4-bit Up Counter (3)



# 4-bit Up Counter (3)





```
`timescale 1 ns/10 ps
module up counter 16 tb;
reg clk;
reg rstn;
wire [3:0] out;
                                                         ⊟up_counter_16 dut (
                                                                    .clock ( ),
                                                               .reset ( ),
                                                                 .out ( )
                                                                     );
always #5 clk = ~clk;
initial
   begin
       // 1. Initialize testbench variables to 0
       clk <= 0;
       rstn <= 0;
       // 2. Drive rest of the stimulus
       #20 rstn <= 1;
      #80 rstn <= 0;
       #50 rstn <= 1;
       // 3. Finish the stimulus after 200ns
       #20 $finish;
   end
endmodule
```

```
`timescale 1 ns/10 ps
 module up counter 16 tb;
 reg clk;
 reg rstn;
 wire [3:0] out;
 // Instantiate counter design .
⊟up counter 16 dut (
            .clock ( ),
            .reset ( ),
            .out ( )
            );
Ę
 always #5 clk = ~clk;
 initial
     begin
// 1. Initialize testbench variables to 0
        clk <= 0;
        rstn <= 0;
        // 2. Drive rest of the stimulus
       #20 rstn <= 1;
       #80 rstn <= 0;
        #50 rstn <= 1;
        // 3. Finish the stimulus after 200ns
         #20 $finish;
     end
 endmodule
```

```
`timescale 1 ns/10 ps
 module up counter 16 tb;
 reg clk;
 reg rstn;
 wire [3:0] out;
 // Instantiate counter design
⊟up counter 16 dut (
             .clock (clk),
             .reset (rstn),
            .out (out)
            );
 always #5 clk = ~clk;
 initial
     begin
         // 1. Initialize testbench variables to 0
         clk <= 0;
        rstn <= 0;
        // 2. Drive rest of the stimulus
        #20 rstn <= 1;
        #80 rstn <= 0;
        #50 rstn <= 1;
         // 3. Finish the stimulus after 200ns
         #20 $finish;
     end
 endmodule
```

Part 2

#### ADD TO WAVE (HOMEWORK)

Part 3

#### **ADD TO LIST**

# Project 1.Directory / 2.Name / 3.Location: counter\_16

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+ mtiUPF	
+	Project Location
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+ modelsim	
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# // Questa	OK Cancel
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# Add Design file only: up\_counter\_16.v

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# Add Design file only: up\_counter\_16.v (2)

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# Add Design file only: up\_counter\_16.v (3)

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# Compile Design file: up\_counter\_16.v

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# Compile Design file: up\_counter\_16.v (2)

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# // All Rights Reserved.
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# // LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //
<pre># reading project counter_10 # reading C:/guestasim64 10.2c/win64//modelsim.ini</pre>
# Loading project counter_16
<pre># Compile of up_counter_16.v was successful.</pre>
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#### **Start Simulation**

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# **Start Simulation (2)**

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# Add to List (different from 'Add to Wave')



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# Add to List (2)



## Force Reset and apply Clock



# Add to List: Force Reset signal to '1'

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# Add to List: Force Reset signal to '1' (2)



# Add to List: Apply Clock signal

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Instance     Design unit     Name	ns-y /up	counter_16/clock			*
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# Add to List: Apply Clock signal (2)



```
# //
# Loading project counter_16
# reading C:/questasim64_10.2c/win64/../modelsim.ini
# Loading project counter_16
# Compile of up_counter_16.v was successful.
QuestaSim> vsim -gui -novopt work.up_counter_16
# vsim -gui -novopt work.up_counter_16
# Refreshing D:/Questasim_projects/counter_16/work.up_counter_16
# Loading work.up_counter_16
add list -r /*
force -freeze sim:/up_counter_16/reset 1'h1 0
force -freeze sim:/up_counter_16/clock 1 0, 0 {25 ns} -r 50
```

VSIM 5>

# **Run Simulation**



## **Result in the First Time and Force Reset to '0'**

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init Name iter_1f dock iter_1f reset	ns-y delta-y	/up_counter_16/clock- /up_counter_16/res /up_counter	et- _16/out
🖪 🖶 🔦 out	0 +0		1 <sup>th1</sup> 4 <sup>thx</sup>
	25 +0	1'h0	1'hl 4'hx
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	75 +0	1'h0	1'h1 4'hx
	100 +0	1'h1	1'hl 4'hx
	125 +0	1'h0	1'hl 4'hx
	150 +0	1'h1	l'hl 4'hx
	175 +0	1'h0	l'hl 4'hx
	200 +0	1'h1	l'hl 4'hx
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# Run Sim again with 400 ns



#### **Result in the Second Time and Force Reset to '1'**

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	200 +1	1'n1 1'n0 4'nx	
	225 +0	1'n0 1'n0 4'nx	
	250 +0	1'h1 1'h0 4'h0	
	275 +0	1'h0 10h0 4'h0	
	300 +0	1'h1 1'h0 4'h0	
	325 +0	1'h0 <mark>1'h0</mark> 4'h0	
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### Run Sim once more with 400 ns



# **Undocking the List window**

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625 +0 1'DU 1201 4'DU		
675 +0 1'h0 1'h1 4'h1		
700 +0 1'h1 1'h1 4'h2		
725 +0 1'h0 1'h1 4'h2		
755 +0 1'h1 1'h1 4'h3		

## List window



## Save Sim Data to a .lst file

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# Save Sim Data to a .lst file (2)

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Libraries						
This PC						Ŧ
Network						<u>}</u>
					2	

# Save Sim Data to sim.lst file



# sim.lst exists in directory 'counter\_16'

#### View

PC → Local Disk (D:) →	Questasim_projects >	counter_16	ٽ ~	Search counter_16		
Name	6	Date modified	Туре	Size		
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Scounter_16.mpf		7/4/2024 7:33 PM	Clip Organizer Me.	. 84 KB		
📔 sim.do		7/3/2024 10:42 PM DO File		1 KB		
📄 sim.lst		7/4/2024 8:48 PM	MASM Listing	3 KB		
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☑ up_counter_16.v	Size: 2.30 KB	3:22 PM	V File	1 KB		
up_counter_16_tb.v	Date modified: 7/4/20	24 8:48 PM :29 PM	V File	1 KB		
vsim.wlf	77	7/4/2024 7:41 PM	WLF File	0 KB		

# Sim Data in sim.lst

🥘 si	m.lst - Notep	ad					
File	Edit Form	at \	/iew Help				
	ns		/up_counter_16/	clock			
	delta		/up_counter_16/reset				
			/up_	_counter_16/out			
	0	+0		1'h1 1'h1 4'hx			
	25	+0		1'h0 1'h1 4'hx			
	50	+0		1 n1 1 n1 4 nx			
	100	+0		1 n0 1 n1 4 nx			
	100	+0		1 n1 1 n1 4 nx			
	125	+0		1'h1 1'h1 4'hx			
	175	+0		1'h0 1'h1 4'hx			
	200	10		1'h1 1'h1 4'hx			
	200	+1		1'h1 1'h0 4'hx			
	225	+0		1'h0 1'h0 4'hx			
	250	+0		1'h1 1'h0 4'h0			
	275	+0		1'h0 1'h0 4'h0			
	300	+0		1'h1 1'h0 4'h0			
	325	+0		1'h0 1'h0 4'h0			
	350	+0		1'h1 1'h0 4'h0			
	375	+0		1'h0 1'h0 4'h0			
	400	+0		1'h1 1'h0 4'h0			
	425	+0		1'h0 1'h0 4'h0			
	450	+0		1'h1 1'h0 4'h0			
	475	+0		1'h0 1'h0 4'h0			
	500	+0		1'h1 1'h0 4'h0			
	525	+0		1'h0 1'h0 4'h0			
	550	+0		1'h1 1'h0 4'h0			
	5/5	+0		1 10 1 10 4 10			
	600	+0		1'h1 1'h1 4'h0			
	625	10		1'h0 1'h1 4'h0			
	650	+0		1'h1 1'h1 4'h1			
	675	+0		1'h0 1'h1 4'h1			
	700	+0		1'h1 1'h1 4'h2			
	725	+0		1'h0 1'h1 4'h2			
	750	+0		1'h1 1'h1 4'h3			
	775	+0		1'h0 1'h1 4'h3			
	800	+0		1'h1 1'h1 4'h4			
	825	+0		1'h0 1'h1 4'h4			
	850	+0		1'h1 1'h1 4'h5			
	875	+0		1'h0 1'h1 4'h5			
	900	+0		1'h1 1'h1 4'h6			
	925	+0	Tuan Nguyen-viet	1'h0 1'h1 4'h6			
	950	+0		1 h1 1 h1 4 h/			
	9/5	+0		1 no 1 n1 4 n/			

# **Thank You**