# Questasim Tutorial
# (GUI/Windows)

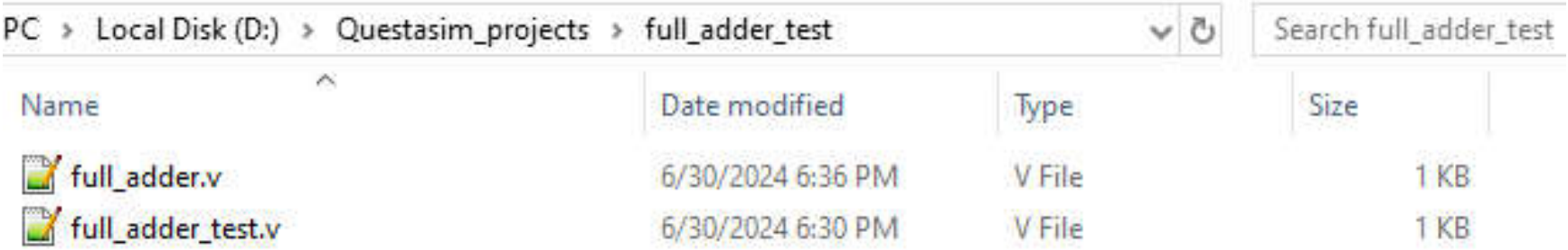
REF: ELEC 5200/6200, Spring 2009, Modelsim Tutorial

# Step 0

- Create a directory for DUT and Test Bench files.
  - E.g.,
    - **D:\Questasim_projects\full_adder_test**

- Write your **Verilog HDL code** in a text editor (e.g., **notepad++**)

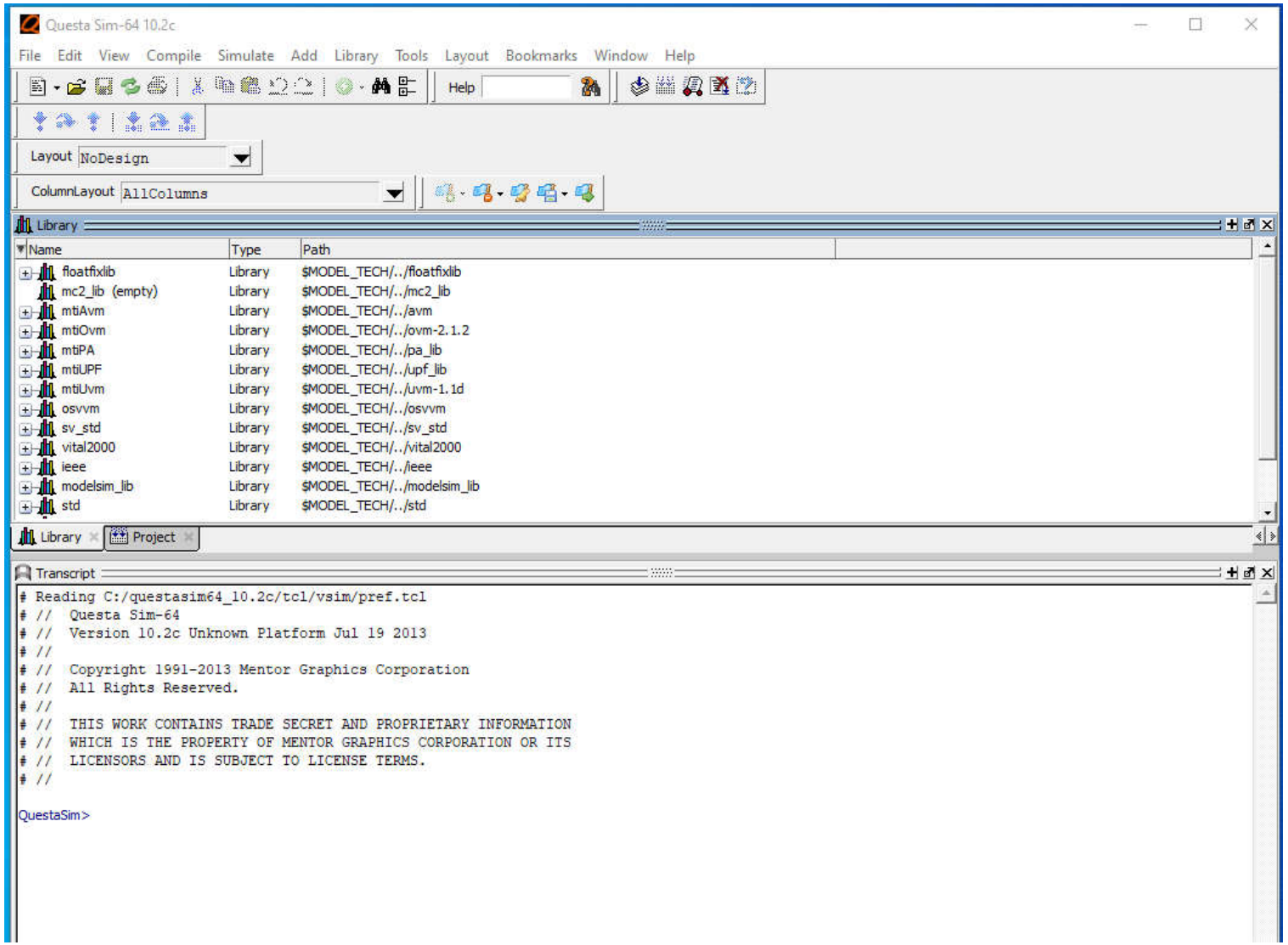
- Save file as **.v files** in the **directory created above**.



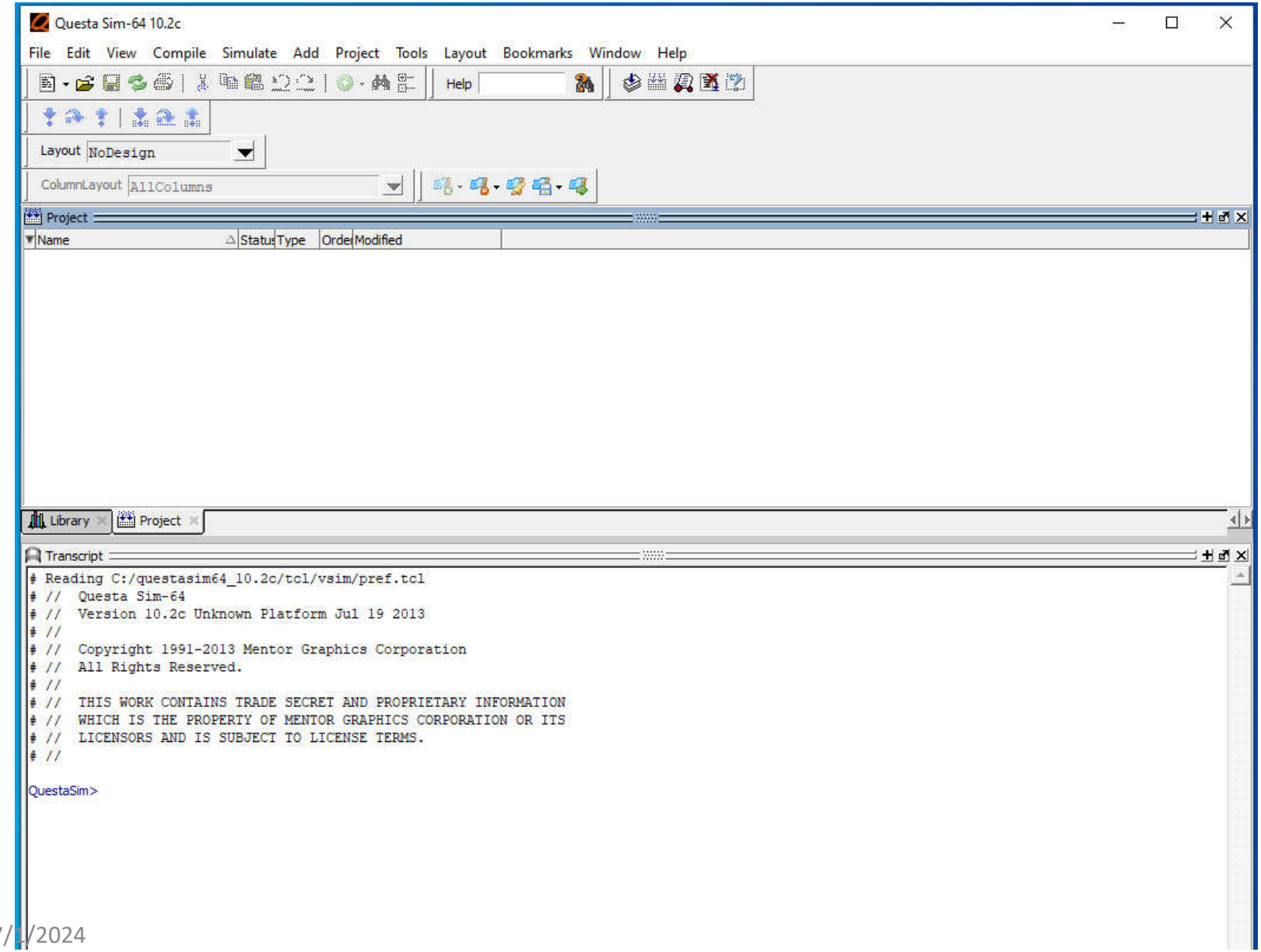
**To simulate using Questasim,**
**follow the steps on the Next Slides.**

# 1

- Start Questasim by double clicking on the icon:

# 1 (bis)


Questa Sim-64 10.2c
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Help
Layout NoDesign
ColumnLayout AllColumns
Project
Name Status Type Order Modified
Library
Project
Transcript
# Reading C:/questasim64_10.2c/tcl/vsim/pref.tcl
# // Questa Sim-64
# // Version 10.2c Unknown Platform Jul 19 2013
# //
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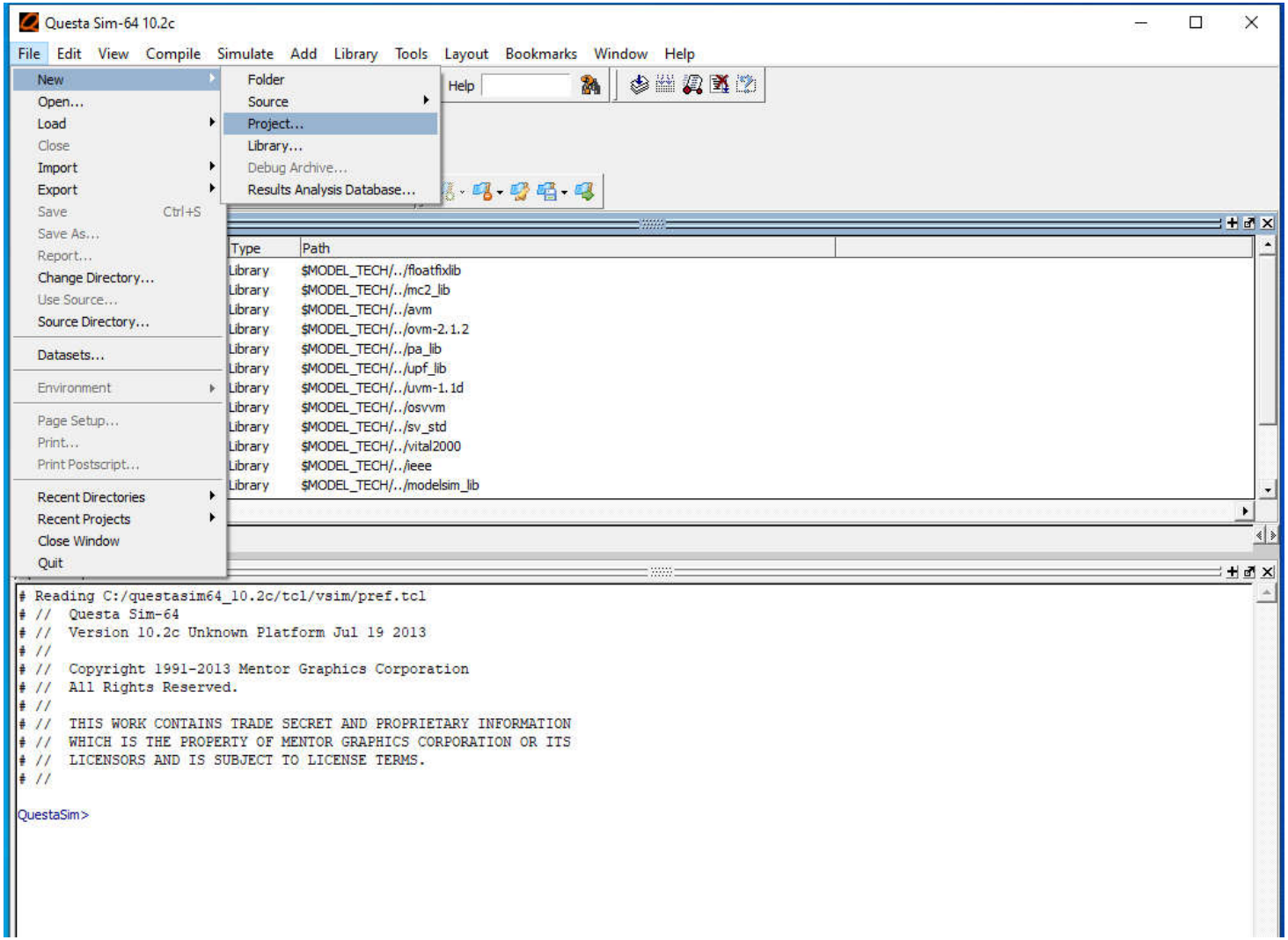
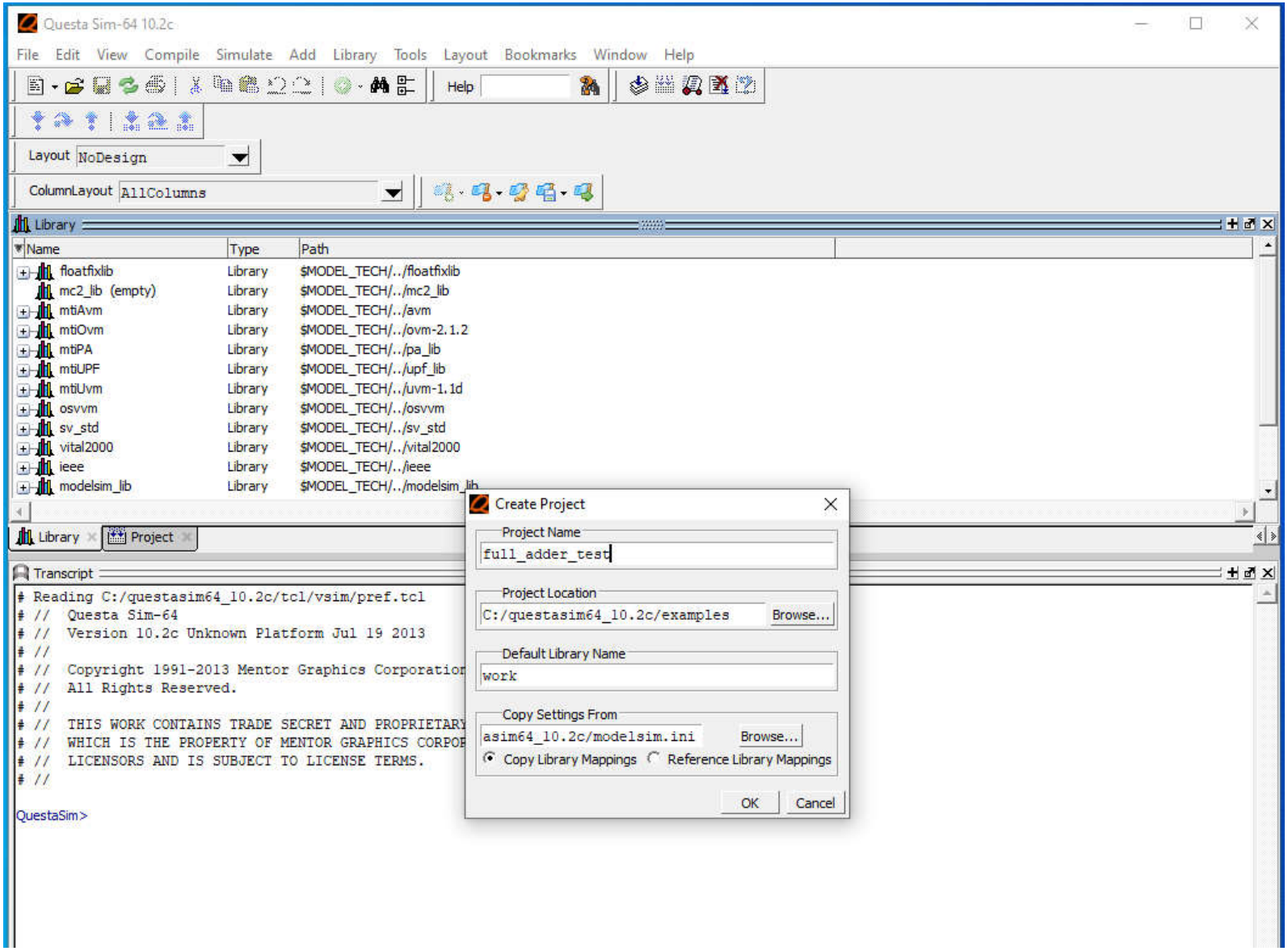
# //
QuestaSim>

# 2

- After starting the Questasim,
  - Create a **New / Project** from the **File** menu as shown in Figure below.

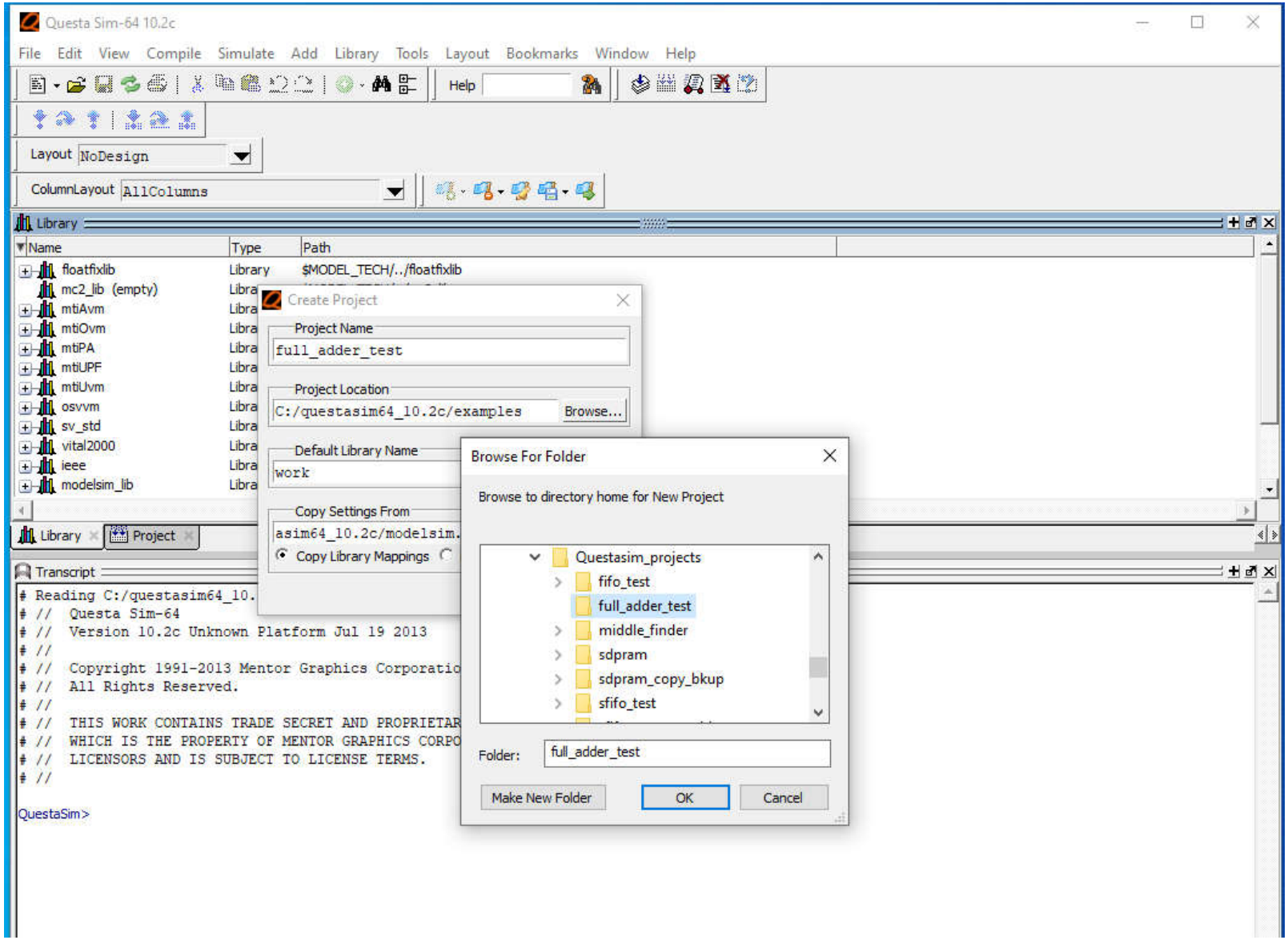


- Give **Project Name** a name. [**full_adder_test**]

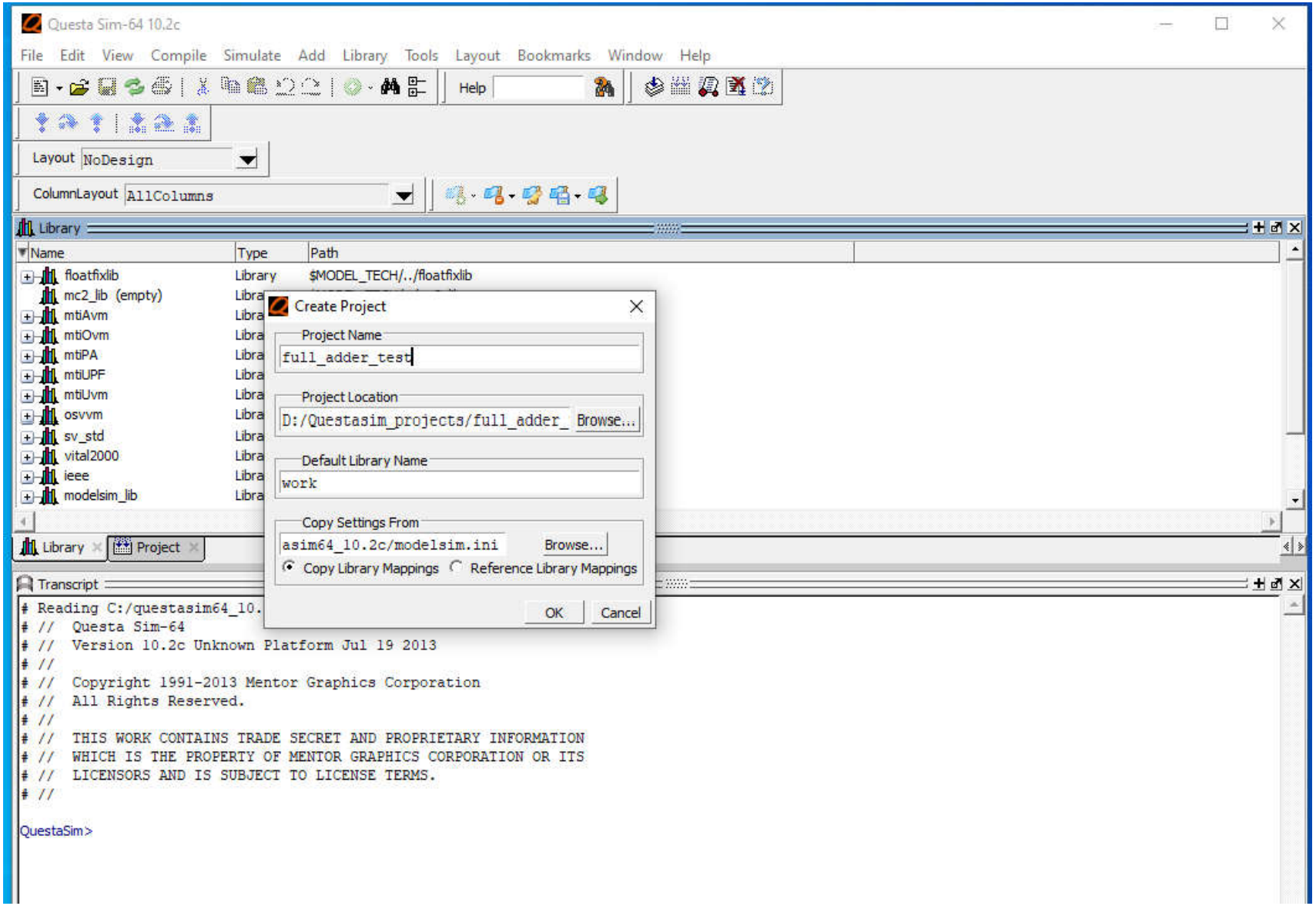


- The **Project Location** is the directory in which you have your Verilog files [**D:\Questasim_projects\full_adder_test**]. Click OK.

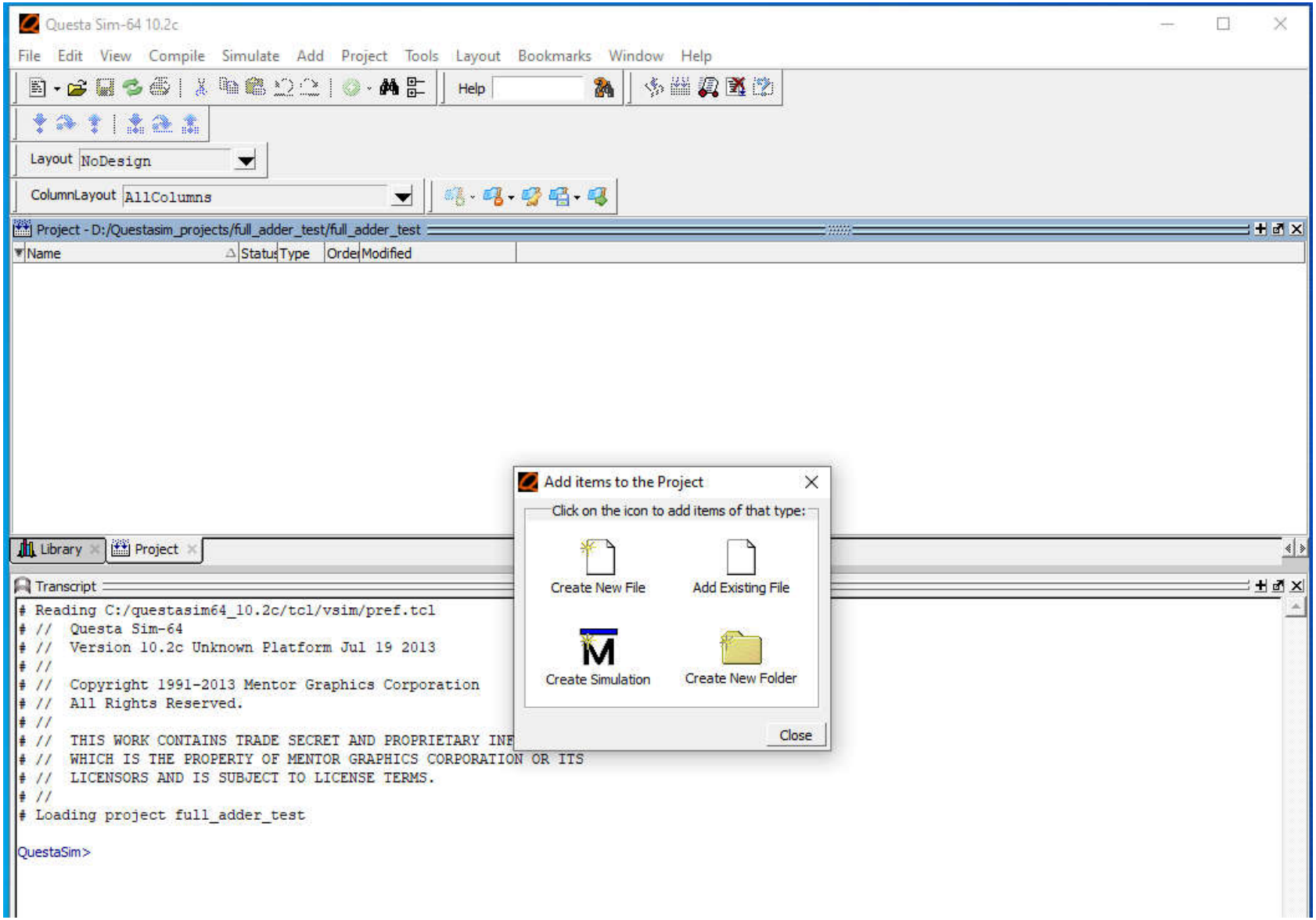




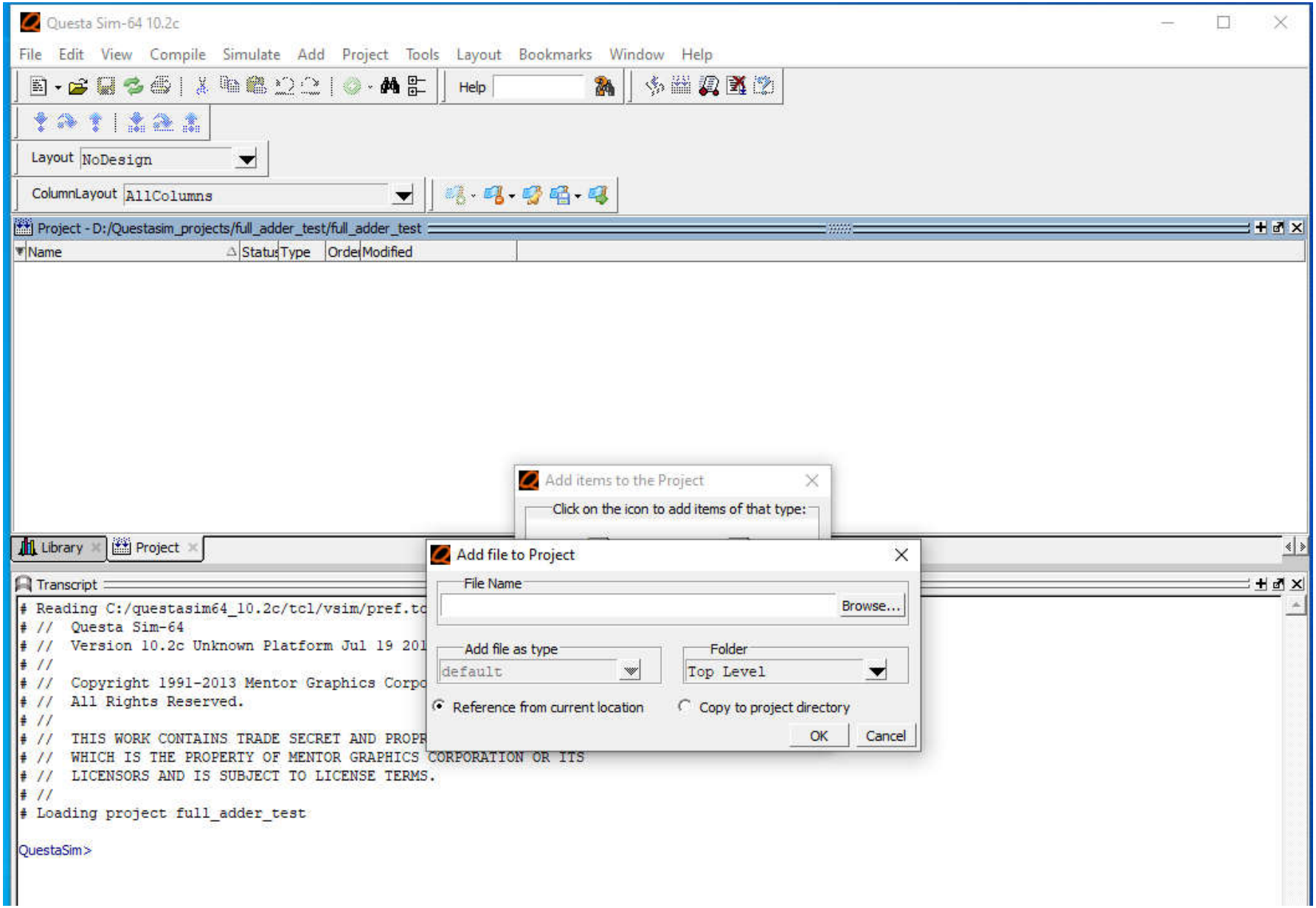
- The **Project Location** [D:\Questasim_projects\full_adder_test] is available. Then click OK.



- After clicking OK, a window, as shown below, will pop up.
- Select **Add Existing File**.



- Brows the Verilog files of the design that you want to simulate.
- Make sure that you select "**Copy to Project Directory**" option. Click OK.



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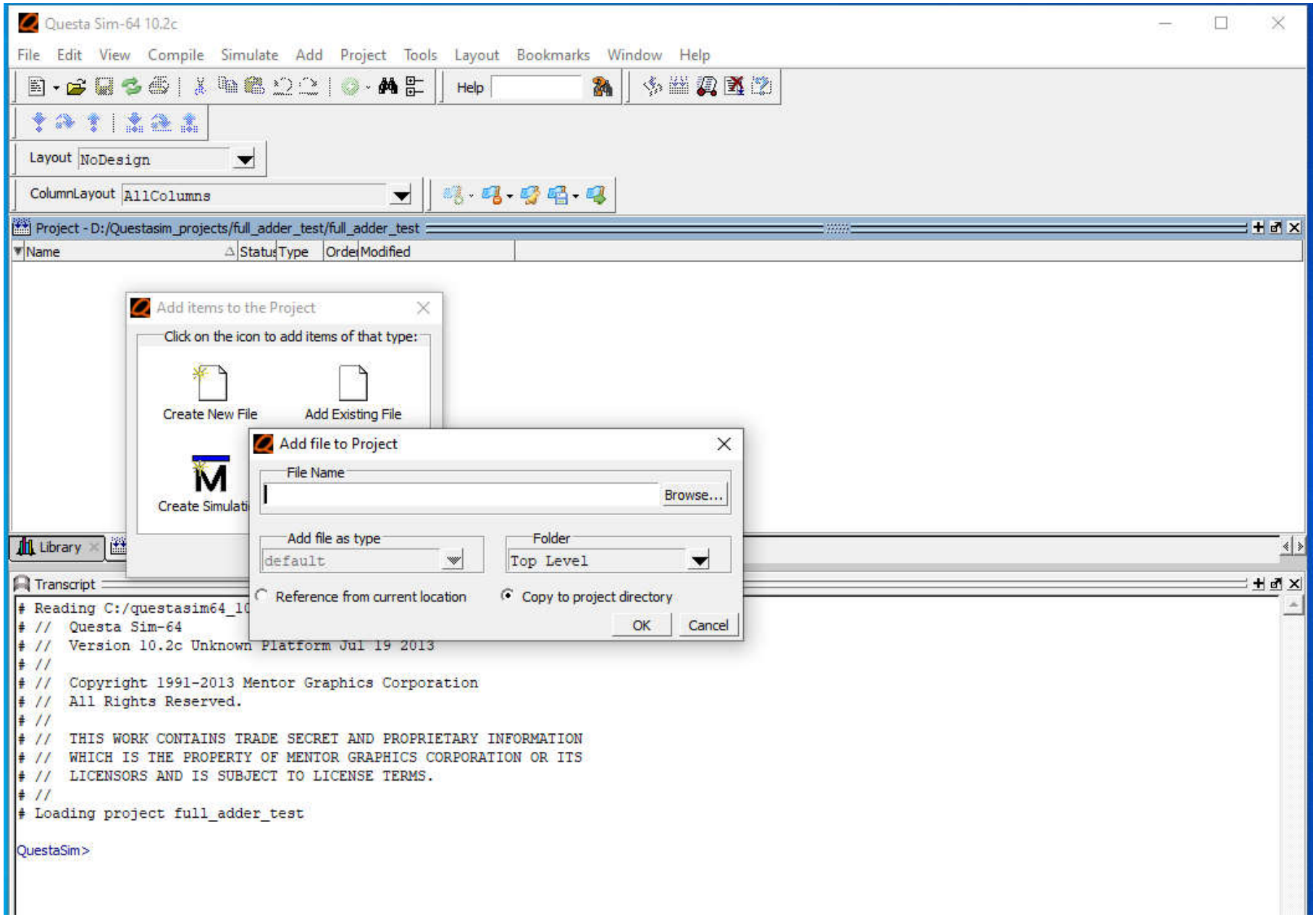

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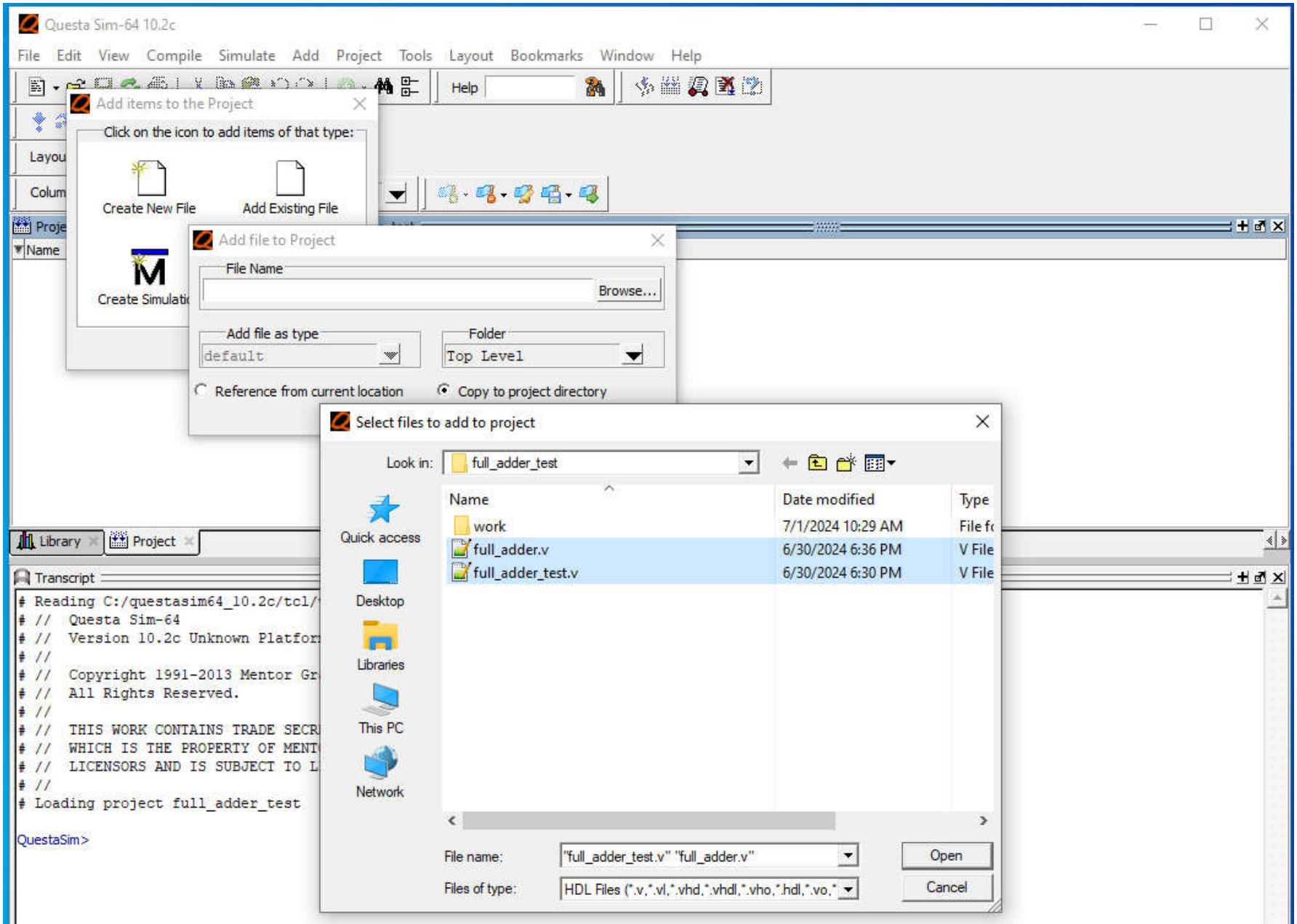
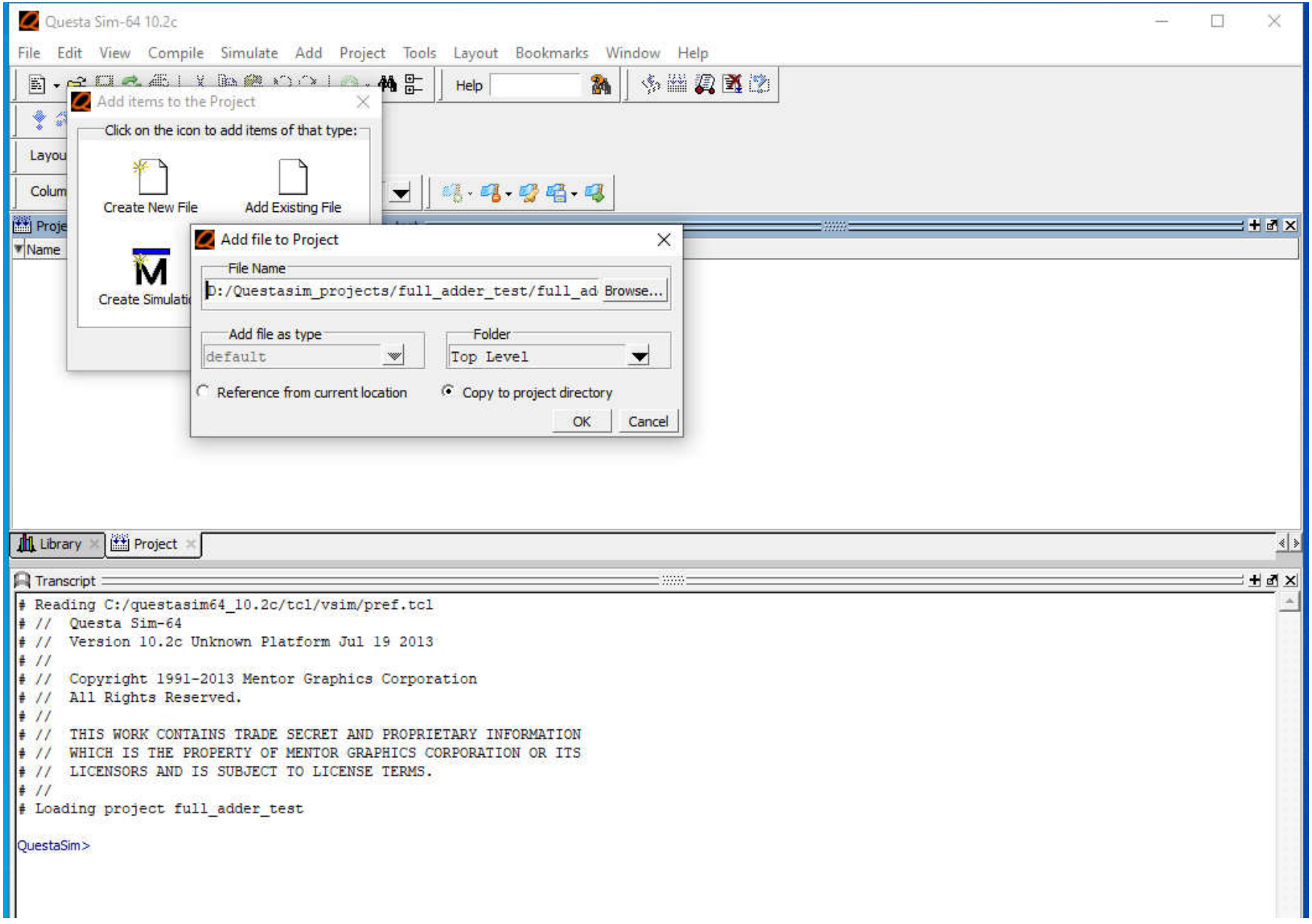
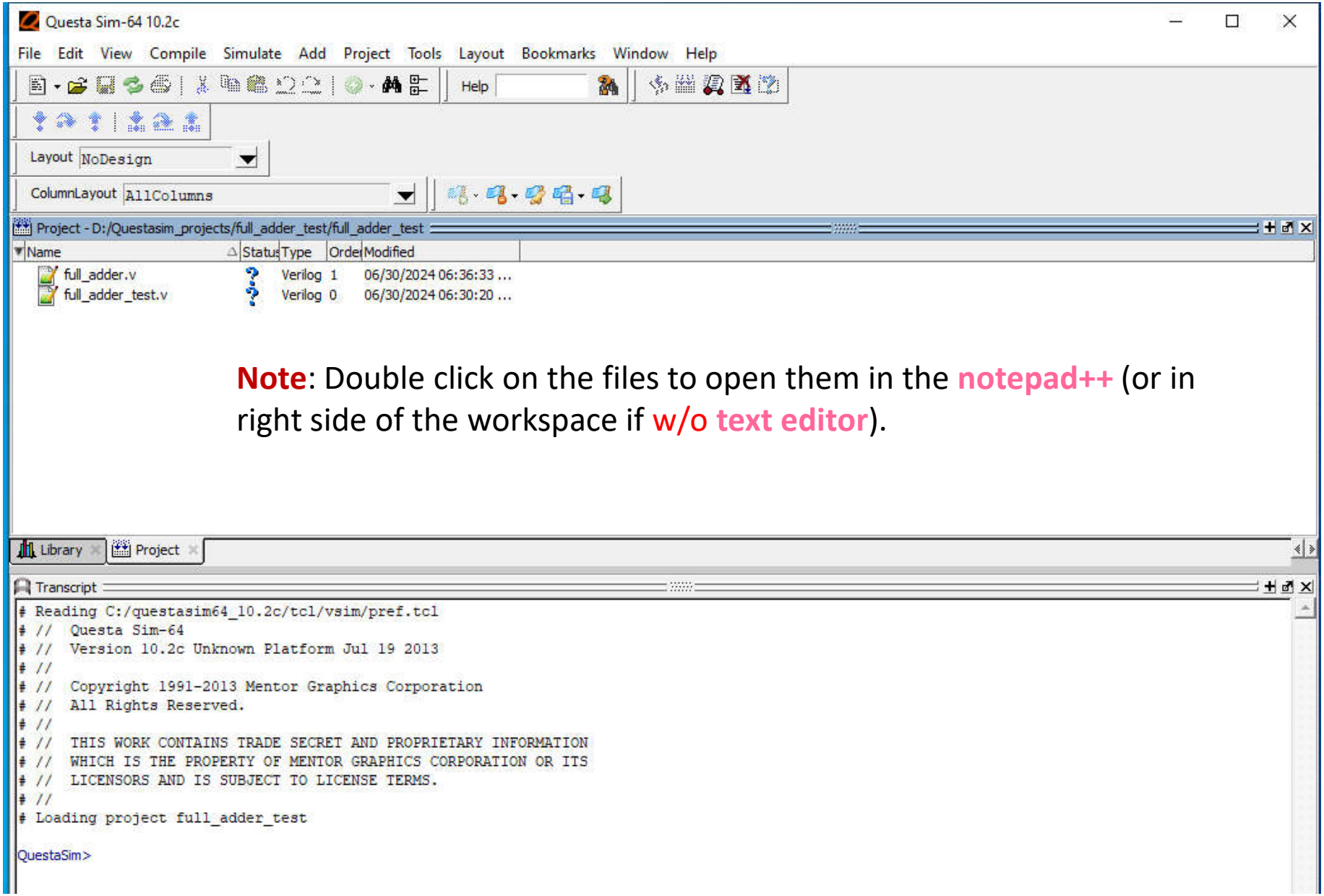


- Brows the Verilog files of the design that you want to simulate.
- Make sure that you select "**Copy to Project Directory**" option. Click OK.

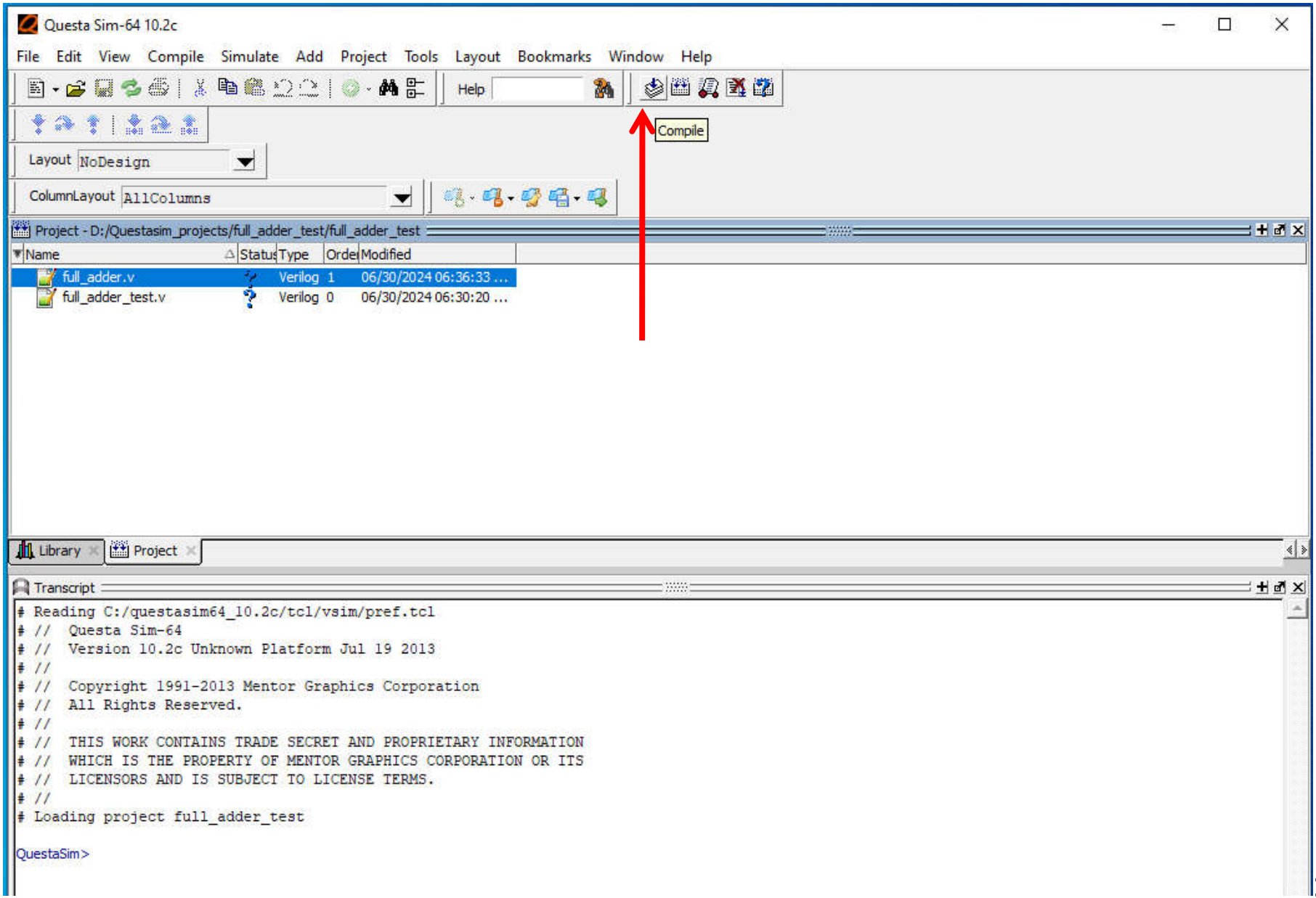


- The selected Verilog files will appear in the workspace (**Project** window).



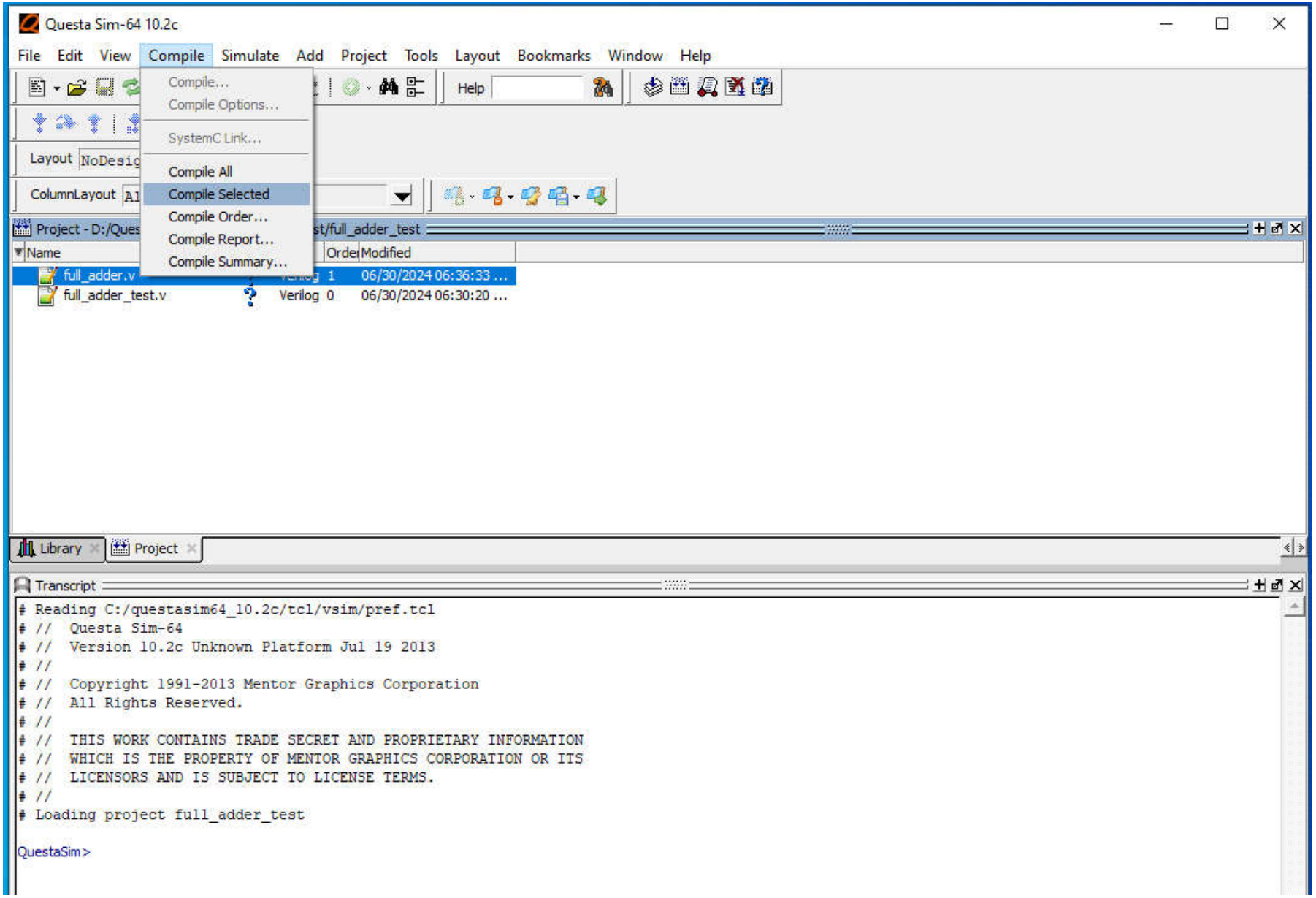

**Note**: Double click on the files to open them in the notepad++ (or in right side of the workspace if w/o text editor).

- Select Verilog file, then click the compile icon at the top as highlighted by red arrow in the figure below and the design will be compiled.



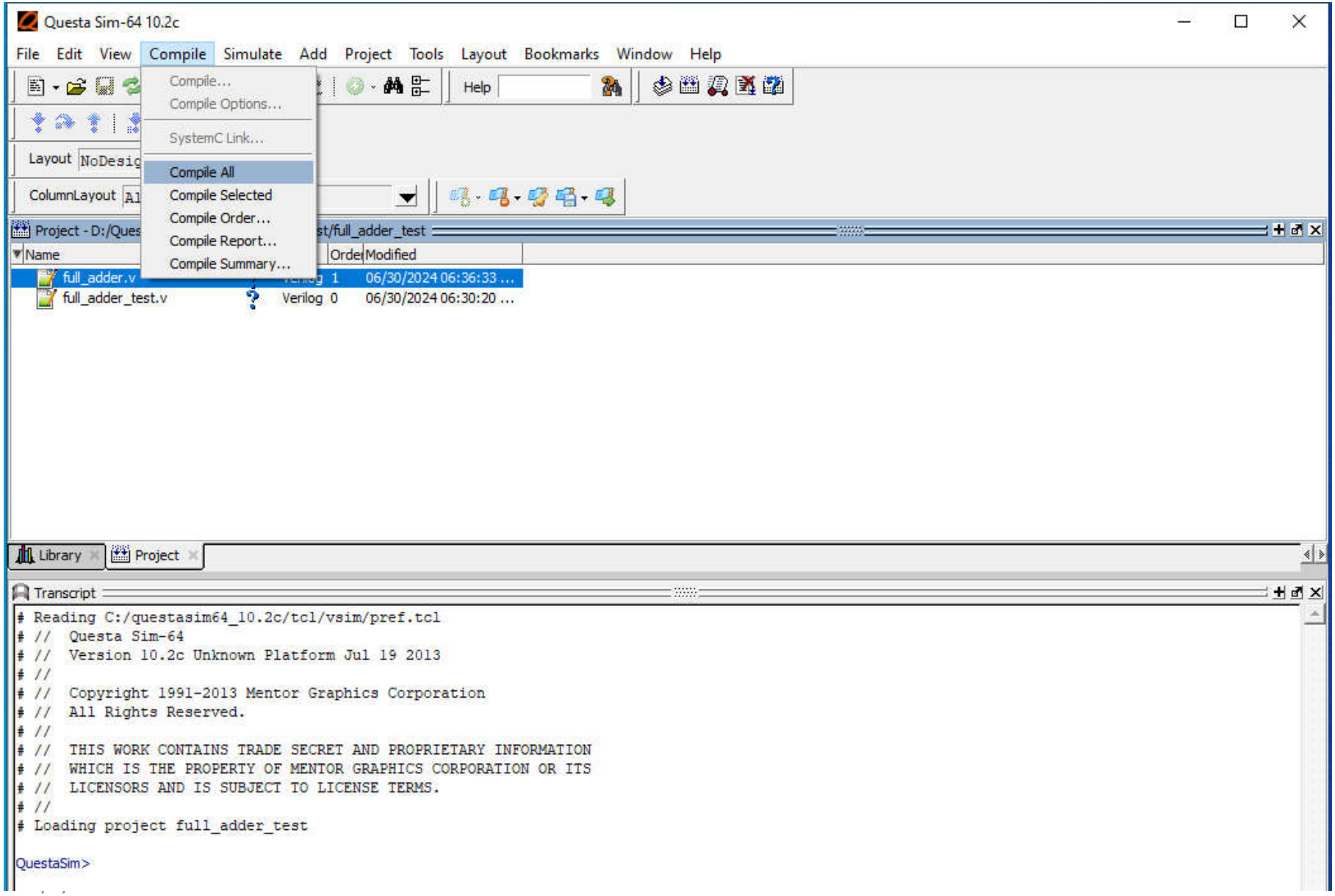
- Select Verilog file, then click the Compile menu at the top as shown in the figure below, choose **Compile Selected** and the design will be compiled.



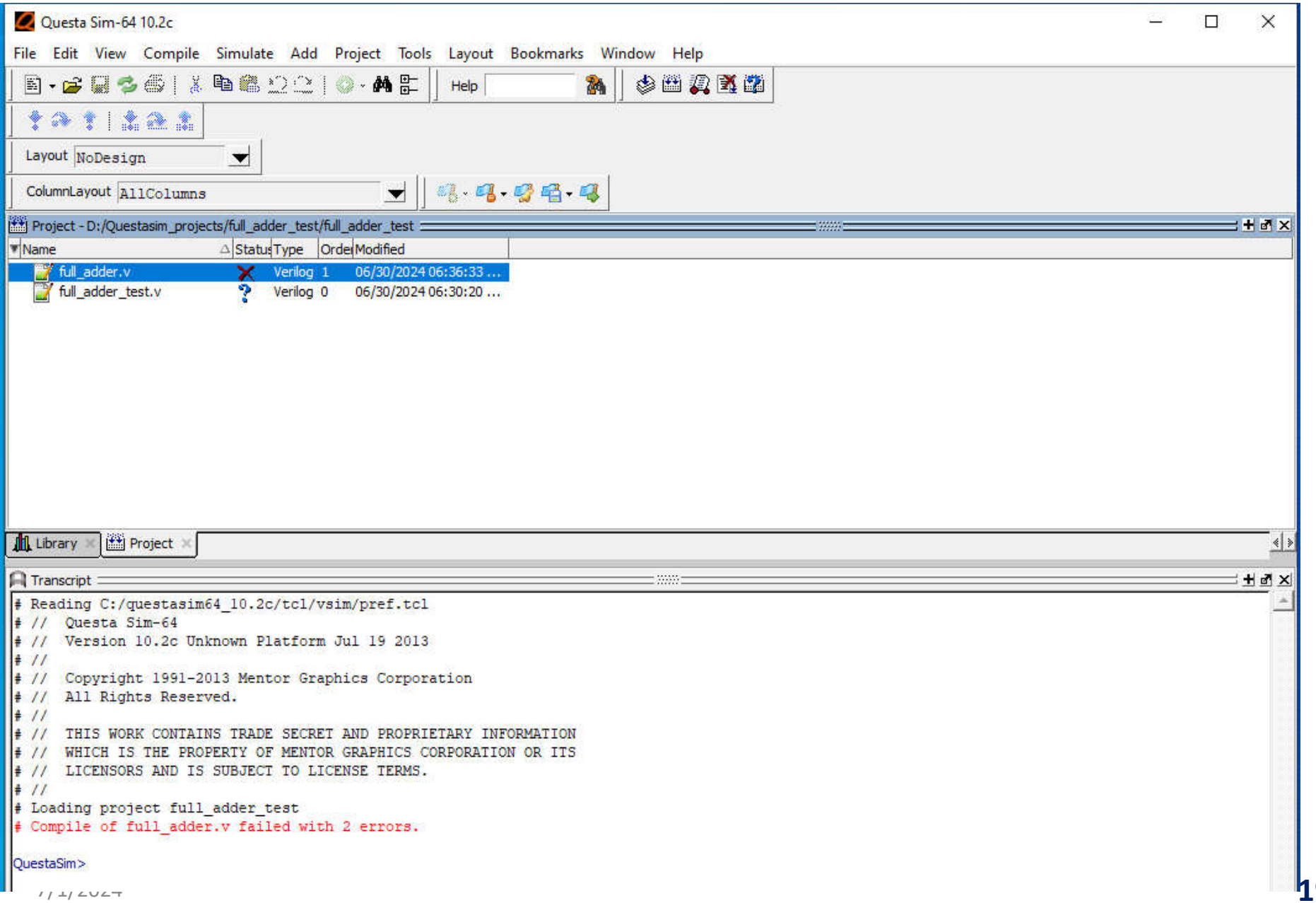


- Or click the Compile menu at the top as shown in the figure below, choose **Compile All** and the design (DUT) and testbench file will be compiled.

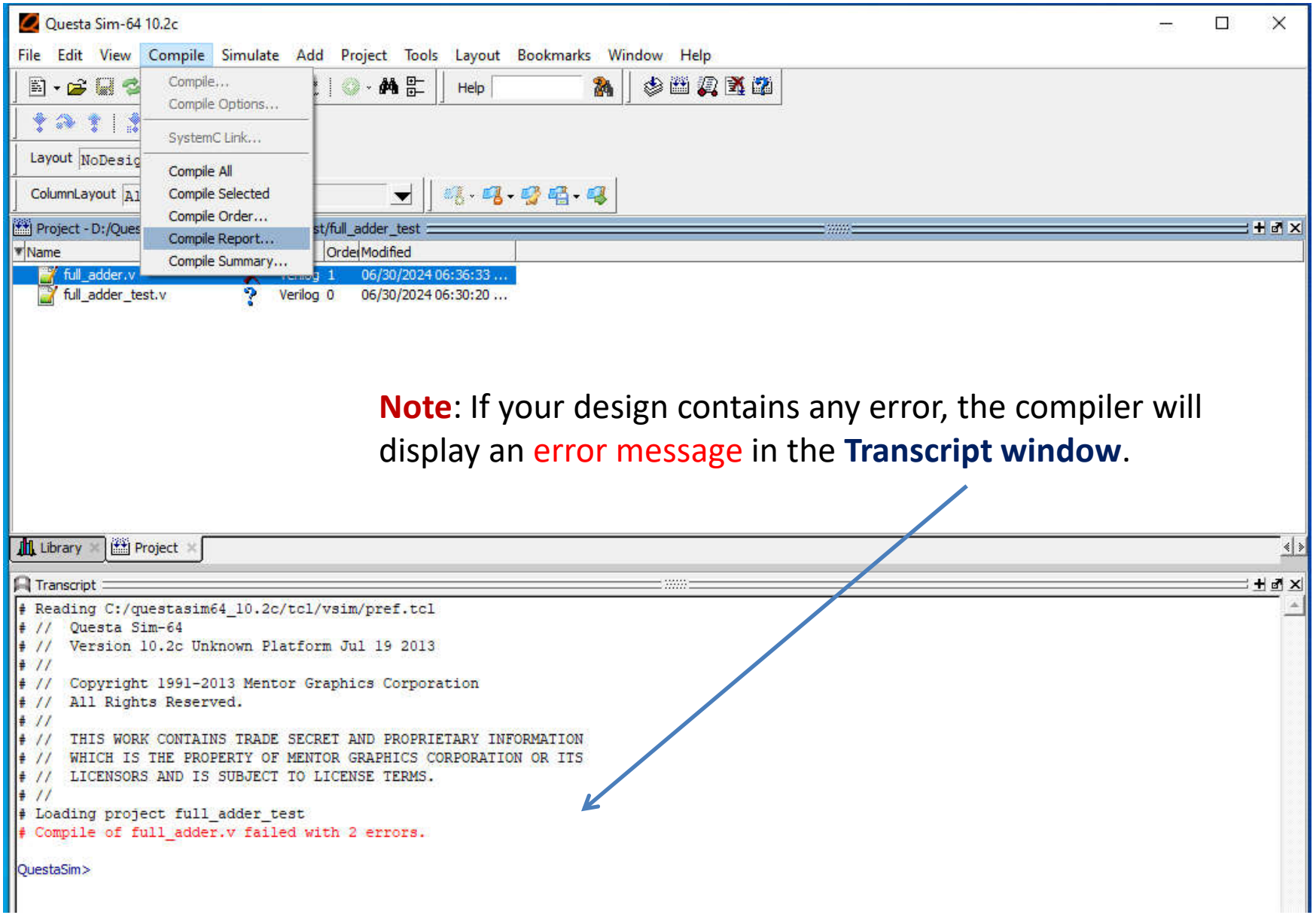




- If errors happen to the design, the tool shows info colored w/ RED line.

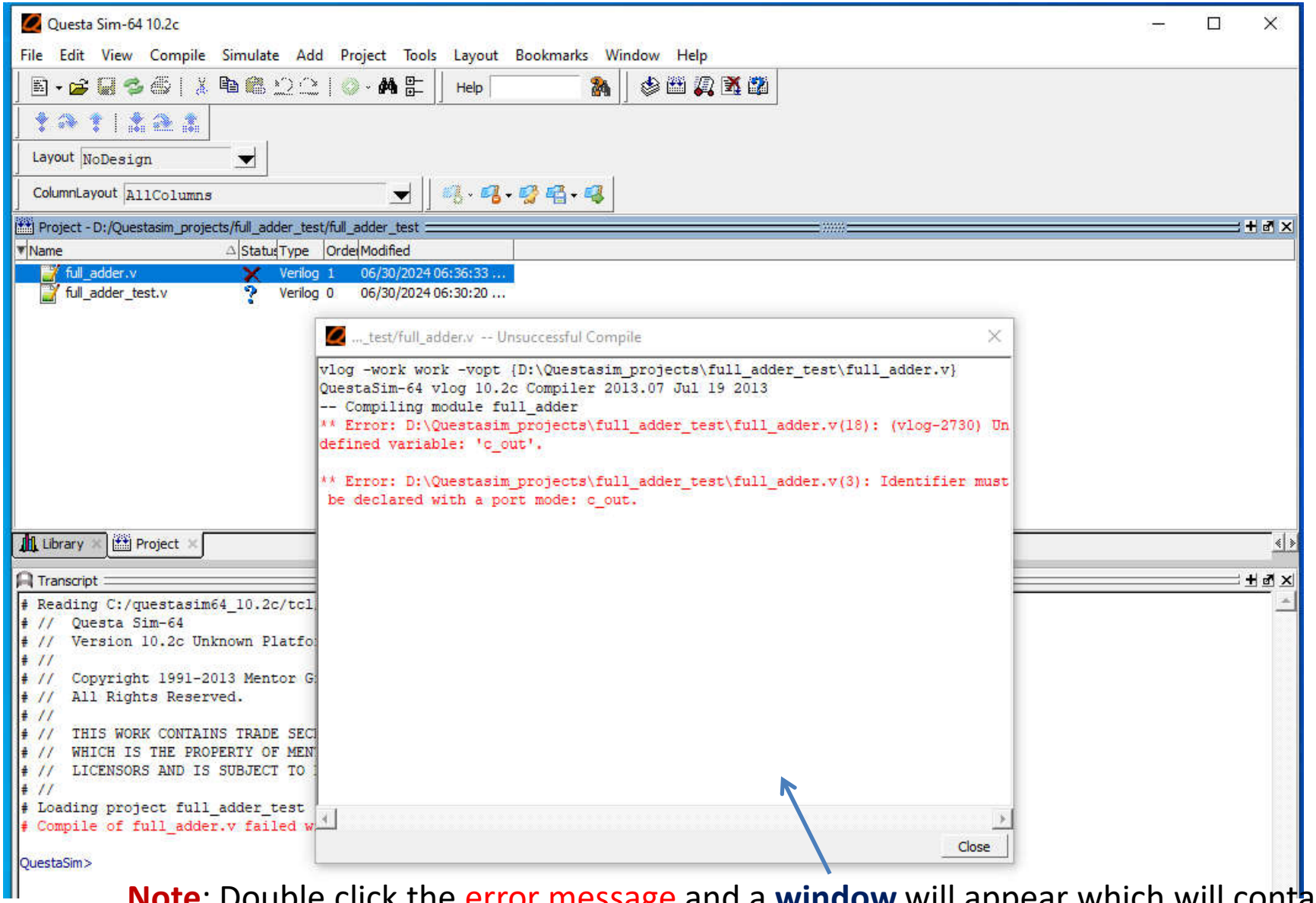


- Select **Compile Report** to see errors.




**Note**: If your design contains any error, the compiler will display an error message in the **Transcript window**.

- Select **Compile Report** to see errors.




**Note**: Double click the error message and a **window** will appear which will contain description of the error and the line no. on which the error has occurred.

- Select **Compile Report** to see errors.

```
3   module full_adder (a_in, b_in, c_in, c_out, sum_out);
4
5   input [3:0] a_in, b_in;
6   input c_in;
7   output carry_out;
8   output [3:0] sum_out;
9
10  reg carry_out;
11  reg [3:0] sum_out;
12
13  always @ (a_in or b_in or c_in)
14      begin
15          {carry_out, sum_out} = a_in + b_in + c_in;
16      end
17
18  endmodule
```

```
3   module full_adder (a_in, b_in, c_in, carry_out, sum_out);
4
5   input [3:0] a_in, b_in;
6   input c_in;
7   output carry_out;
8   output [3:0] sum_out;
9
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14      begin
15          {carry_out, sum_out} = a_in + b_in + c_in;
16      end
17
18  endmodule
```

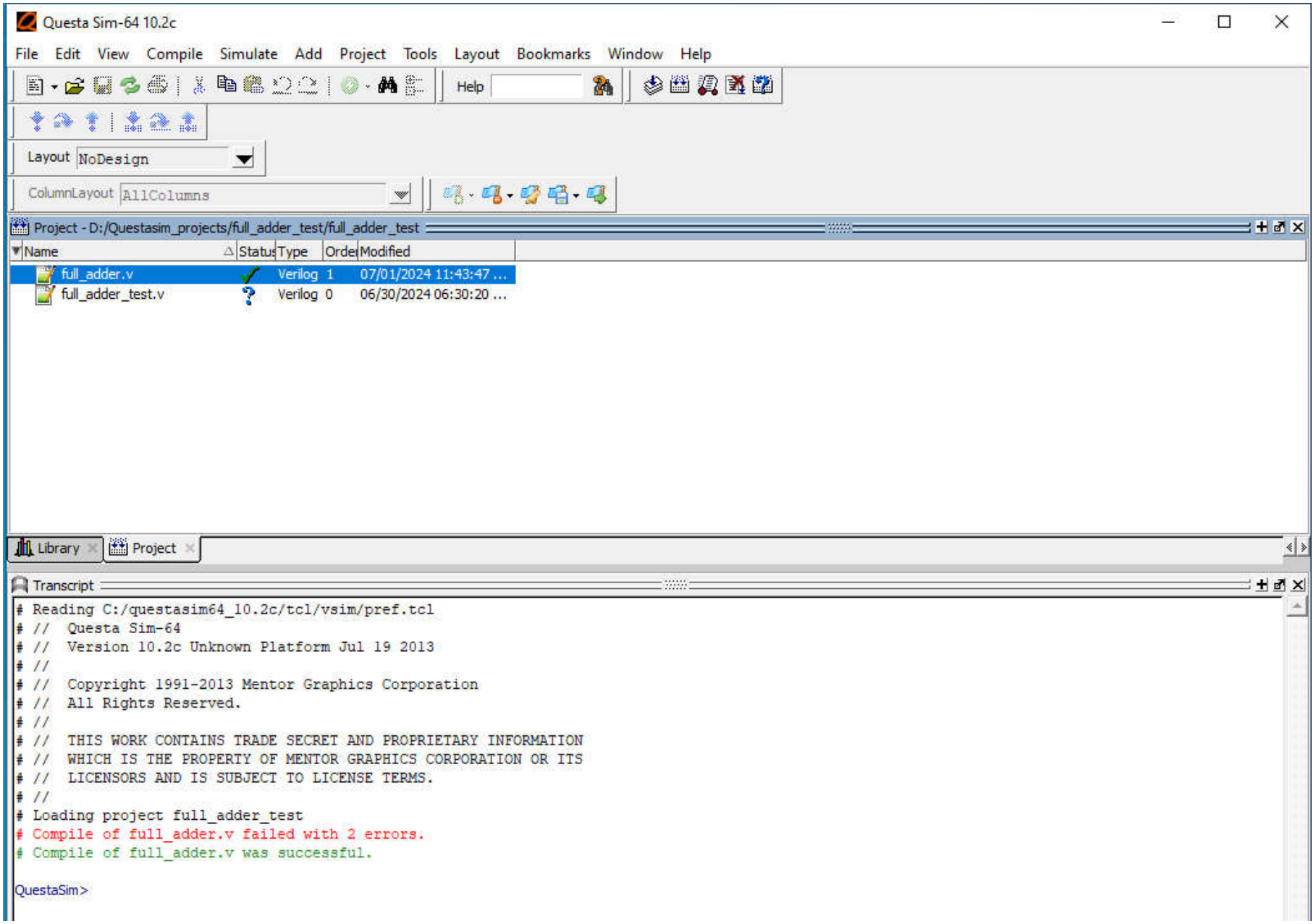
Questa Sim-64 10.2c
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Help
Layout NoDesign
ColumnLayout AllColumns
Project - D:/Questasim_projects/full_adder_test/full_adder_test
Name Status Type Order Modified
full_adder.v Verilog 1 07/01/2024 11:43:47 ...
full_adder_test.v Verilog 0 06/30/2024 06:30:20 ...
Library
Project
Transcript
# Reading C:/questasim64_10.2c/tcl/vsim/pref.tcl
# // Questa Sim-64
# // Version 10.2c Unknown Platform Jul 19 2013
# //
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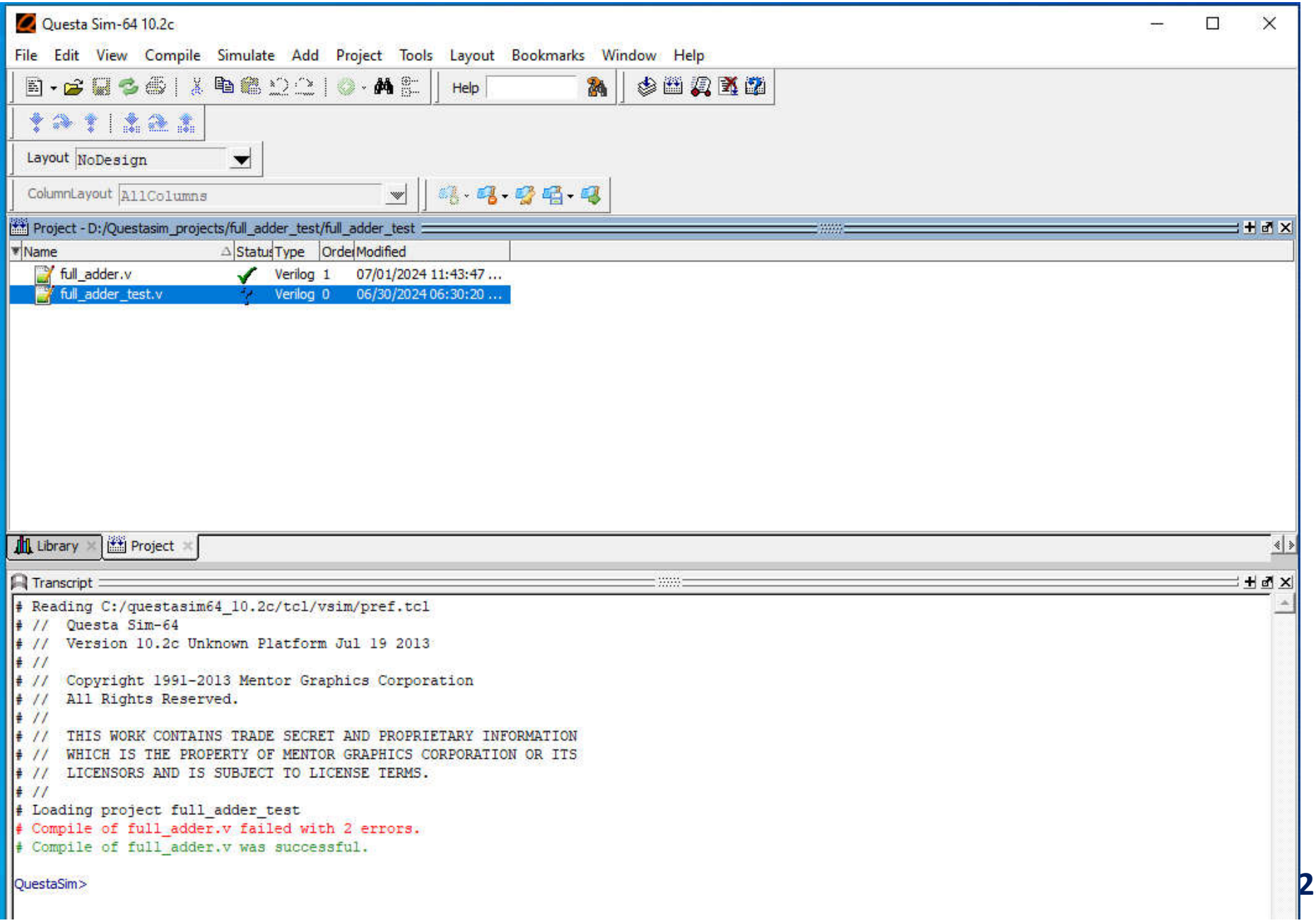
# //
# Loading project full_adder_test
# Compile of full_adder.v failed with 2 errors.
# Compile of full_adder.v was successful.
QuestaSim>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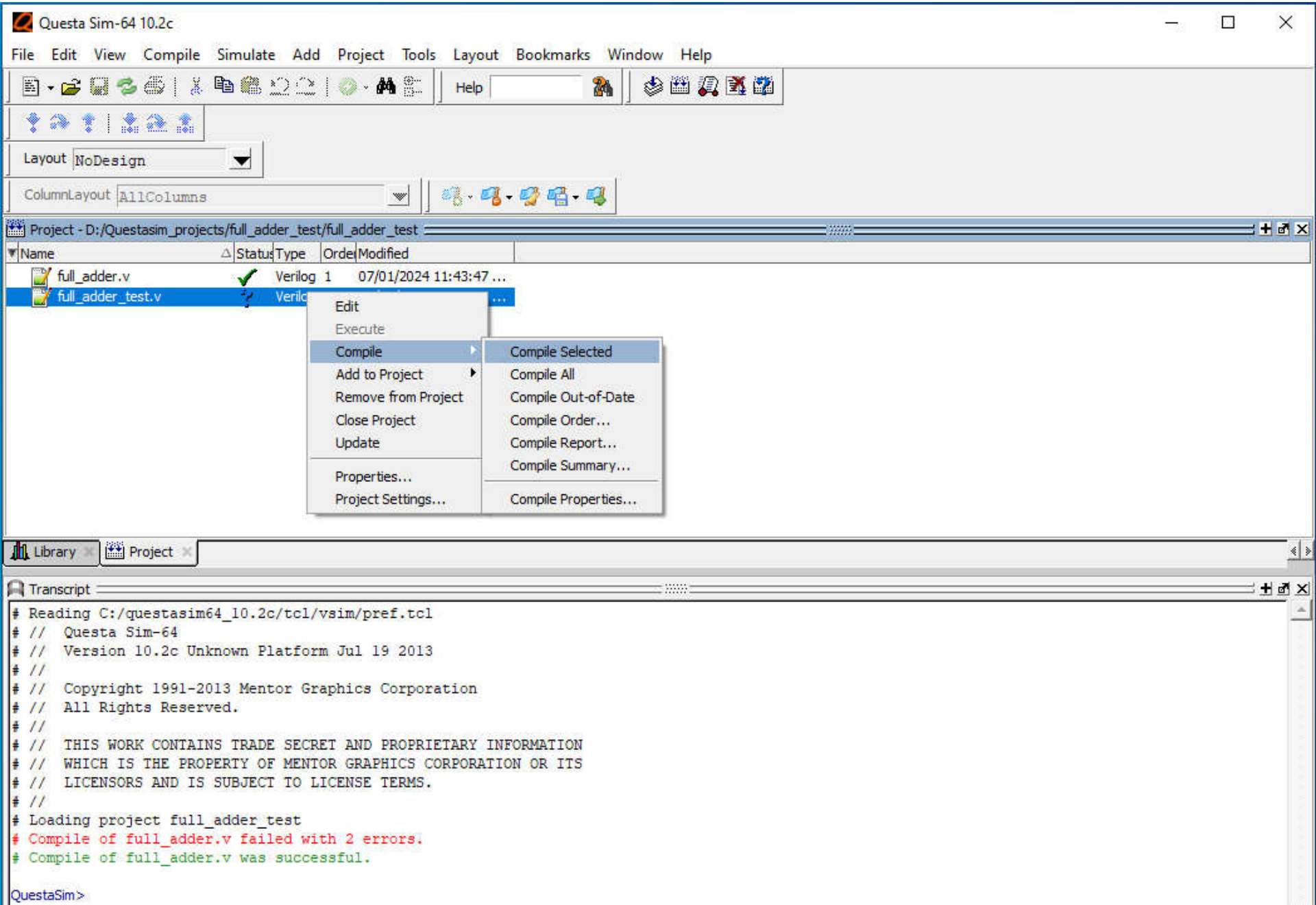
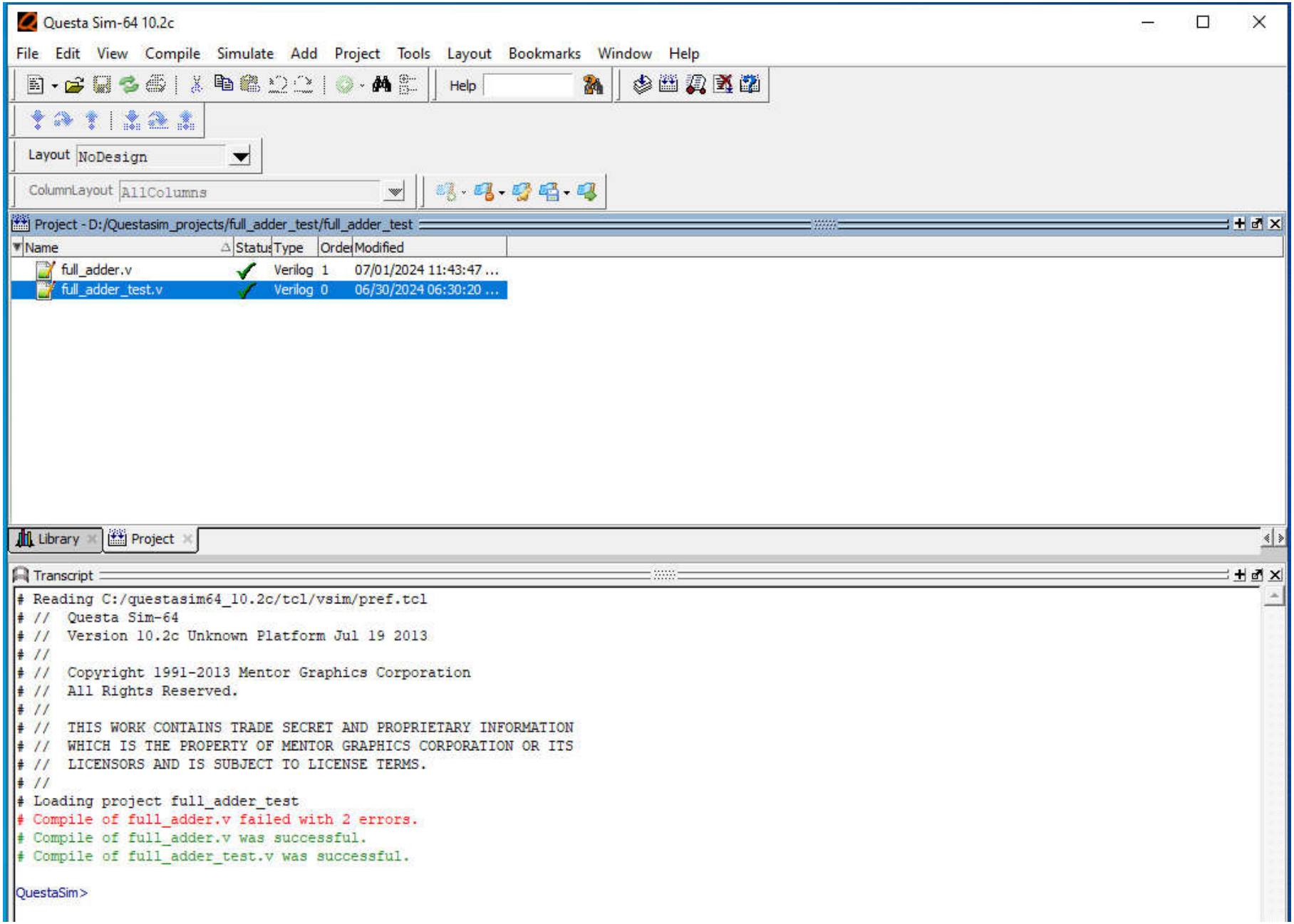
# //
# Loading project full_adder_test
# Compile of full_adder.v failed with 2 errors.
# Compile of full_adder.v was successful.
QuestaSim>

- Double click on **full_adder_test.v** file, choose **Compile Selected** to run…



- … Successful


Questa Sim-64 10.2c
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Help
Layout NoDesign
ColumnLayout AllColumns
Project - D:/Questasim_projects/full_adder_test/full_adder_test
Name Status Type Order Modified
full_adder.v Verilog 1 07/01/2024 11:43:47 ...
full_adder_test.v Verilog 0 06/30/2024 06:30:20 ...
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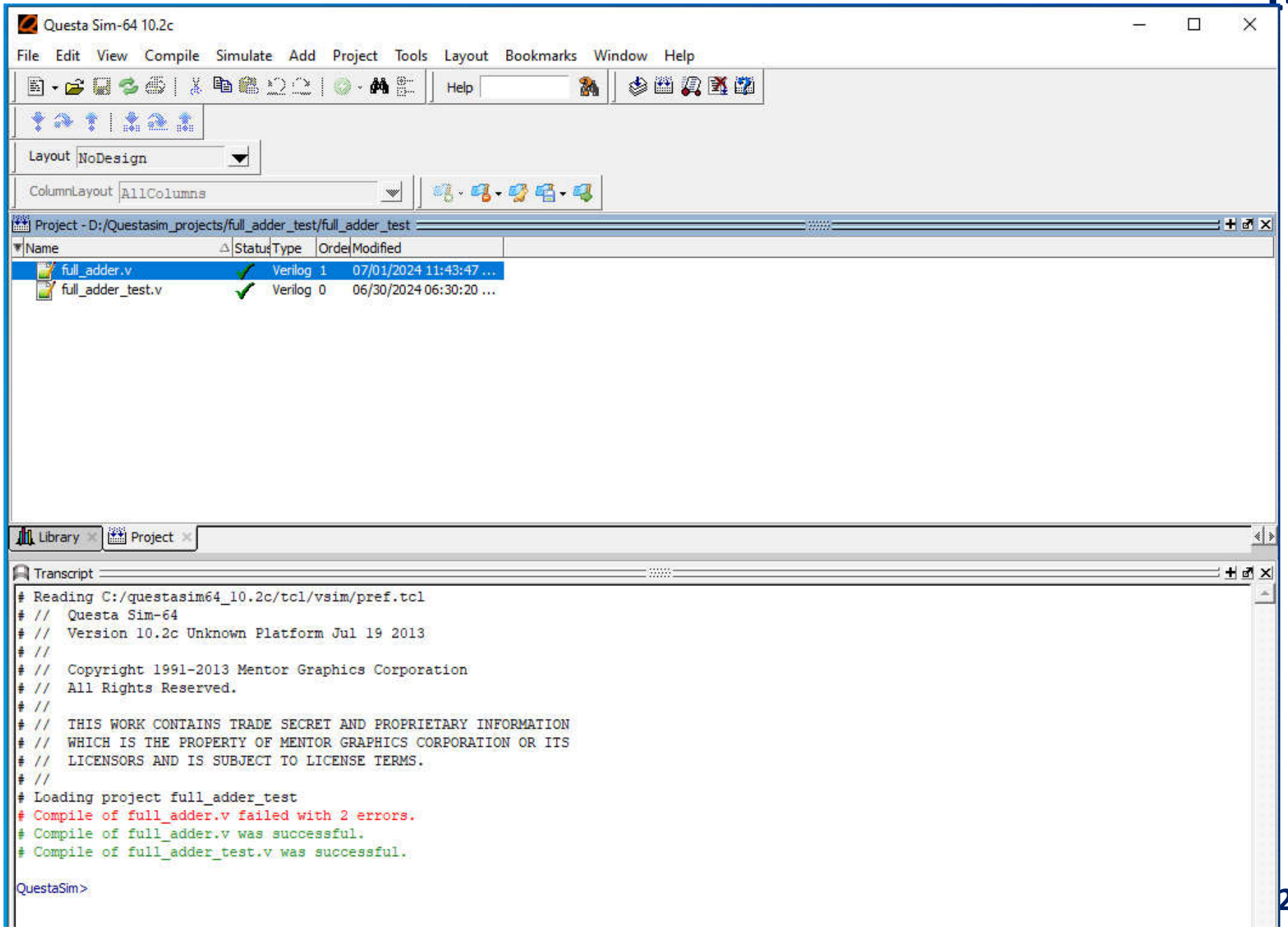
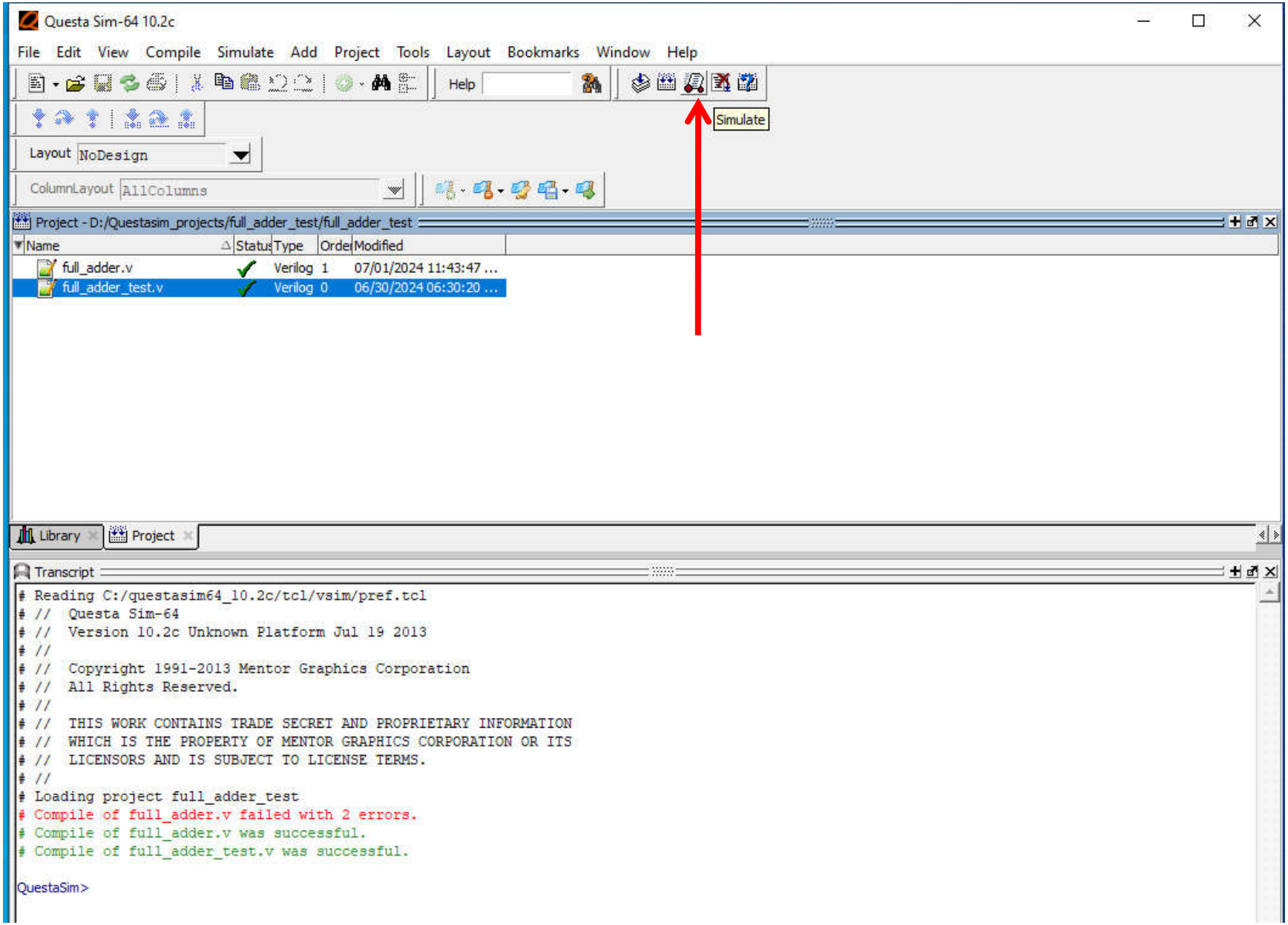
# //
# Loading project full_adder_test
# Compile of full_adder.v failed with 2 errors.
# Compile of full_adder.v was successful.
# Compile of full_adder_test.v was successful.
QuestaSim>

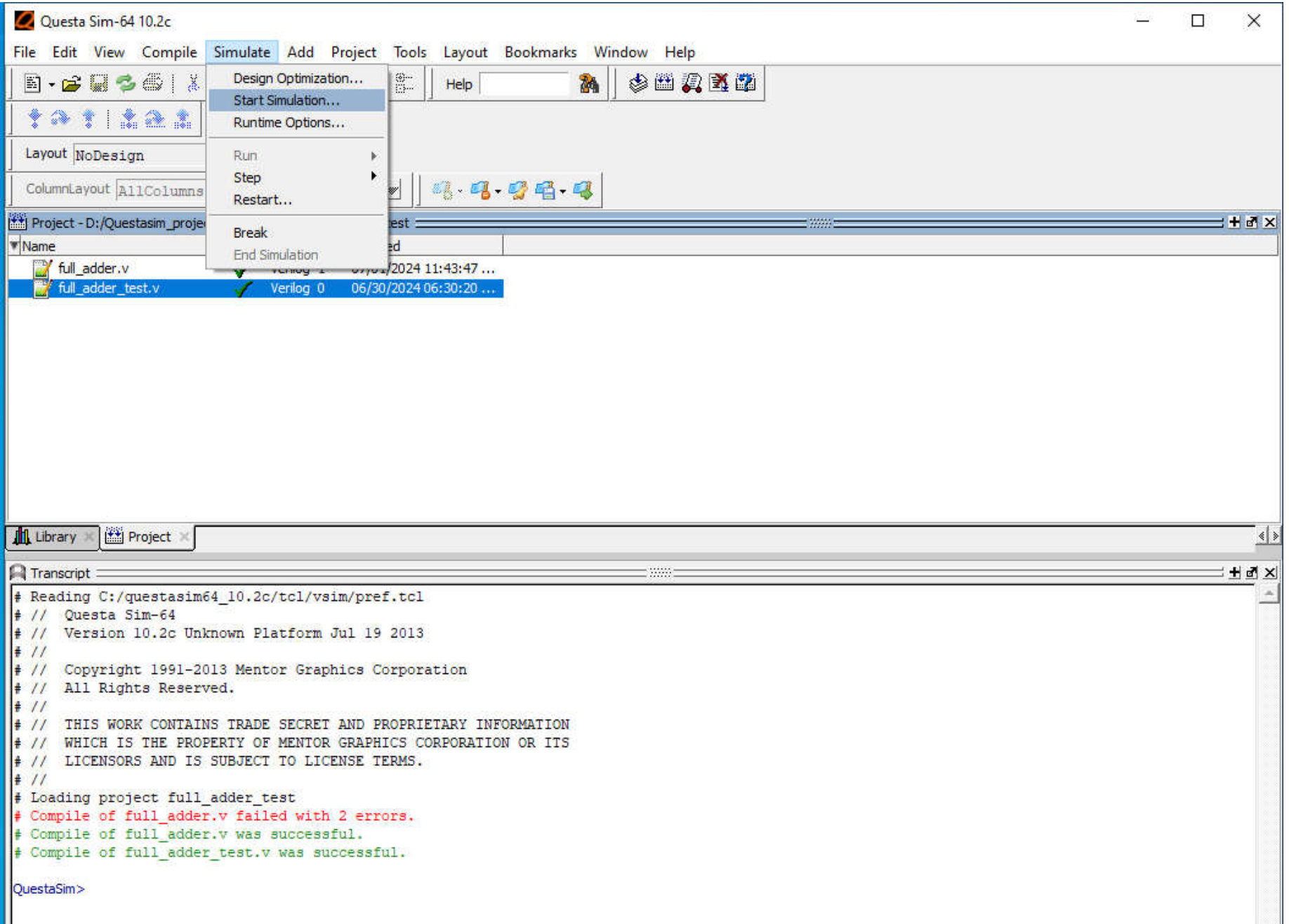
- … Successful Compilation.



After compilation is successful,

- we **simulate** the design using an icon highlighted by RED arrow in figure.




Questa Sim-64 10.2c
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Design Optimization...
Start Simulation...
Runtime Options...
Run
Step
Restart...
Break
End Simulation
Help
Layout NoDesign
ColumnLayout AllColumns
Project - D:/Questasim_proje
Name
full_adder.v
full_adder_test.v
Verilog 0
06/30/2024 06:30:20 ...
Library
Project
Transcript
# Reading C:/questasim64_10.2c/tcl/vsim/pref.tcl
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# Loading project full_adder_test
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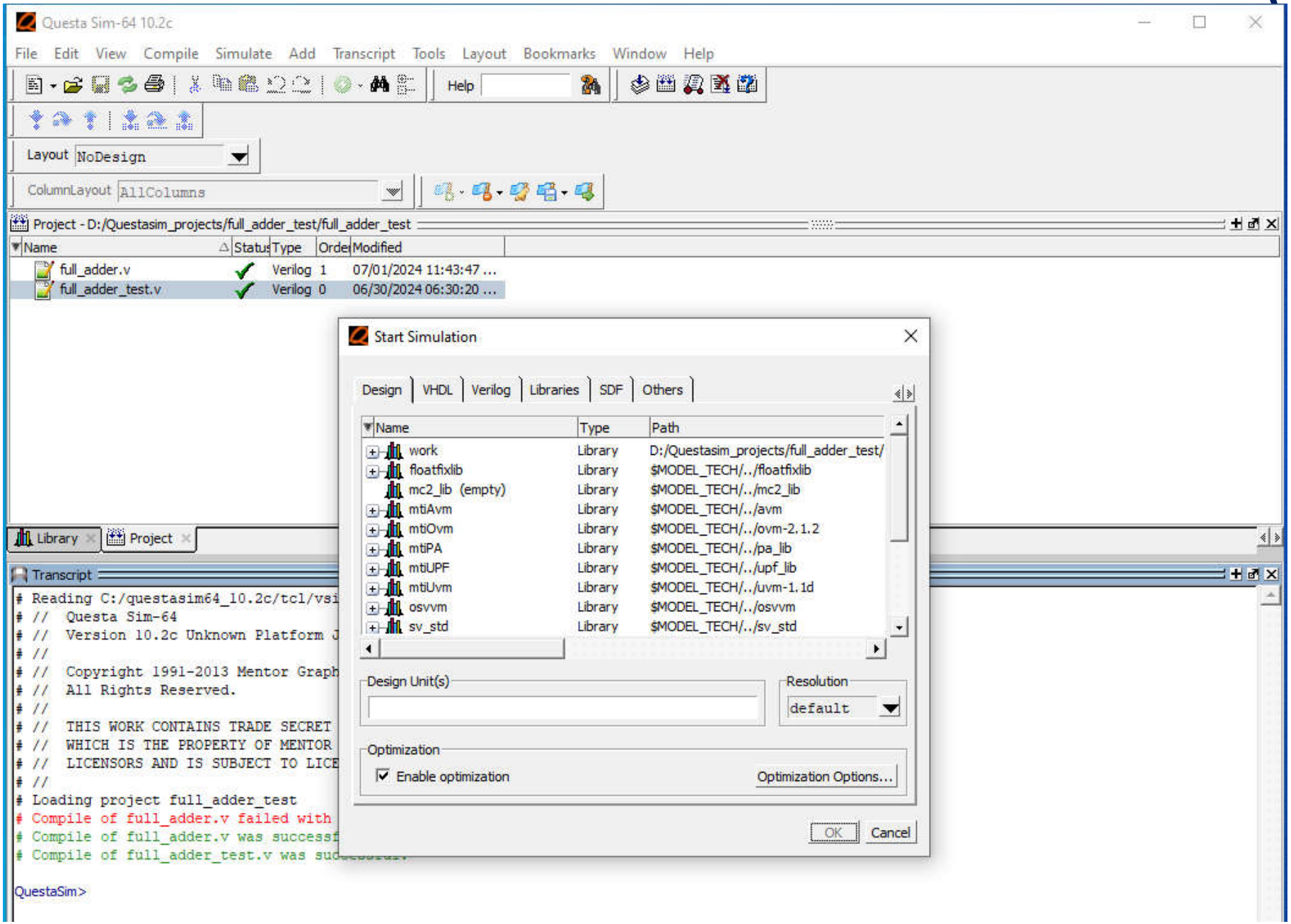
Questa Sim-64 10.2c
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
Help
Layout NoDesign
ColumnLayout AllColumns
Project - D:/Questasim_projects/full_adder_test/full_adder_test
Name Status Type Order Modified
full_adder.v Verilog 1 07/01/2024 11:43:47 ...
full_adder_test.v Verilog 0 06/30/2024 06:30:20 ...
Start Simulation
Design VHDL Verilog Libraries SDF Others
Name Type Path
work Library D:/Questasim_projects/full_adder_test/
floatfixlib Library $MODEL_TECH/../floatfixlib
mc2_lib (empty) Library $MODEL_TECH/../mc2_lib
mtiAvm Library $MODEL_TECH/../avm
mtiOvm Library $MODEL_TECH/../ovm-2.1.2
mtiPA Library $MODEL_TECH/../pa_lib
mtiUPF Library $MODEL_TECH/../upf_lib
mtiUvm Library $MODEL_TECH/../uvm-1.1d
osvvm Library $MODEL_TECH/../osvvm
sv_std Library $MODEL_TECH/../sv_std
Design Unit(s)
Resolution
default
Optimization
Enable optimization
Optimization Options...
OK
Cancel
Library
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# // Questa Sim-64
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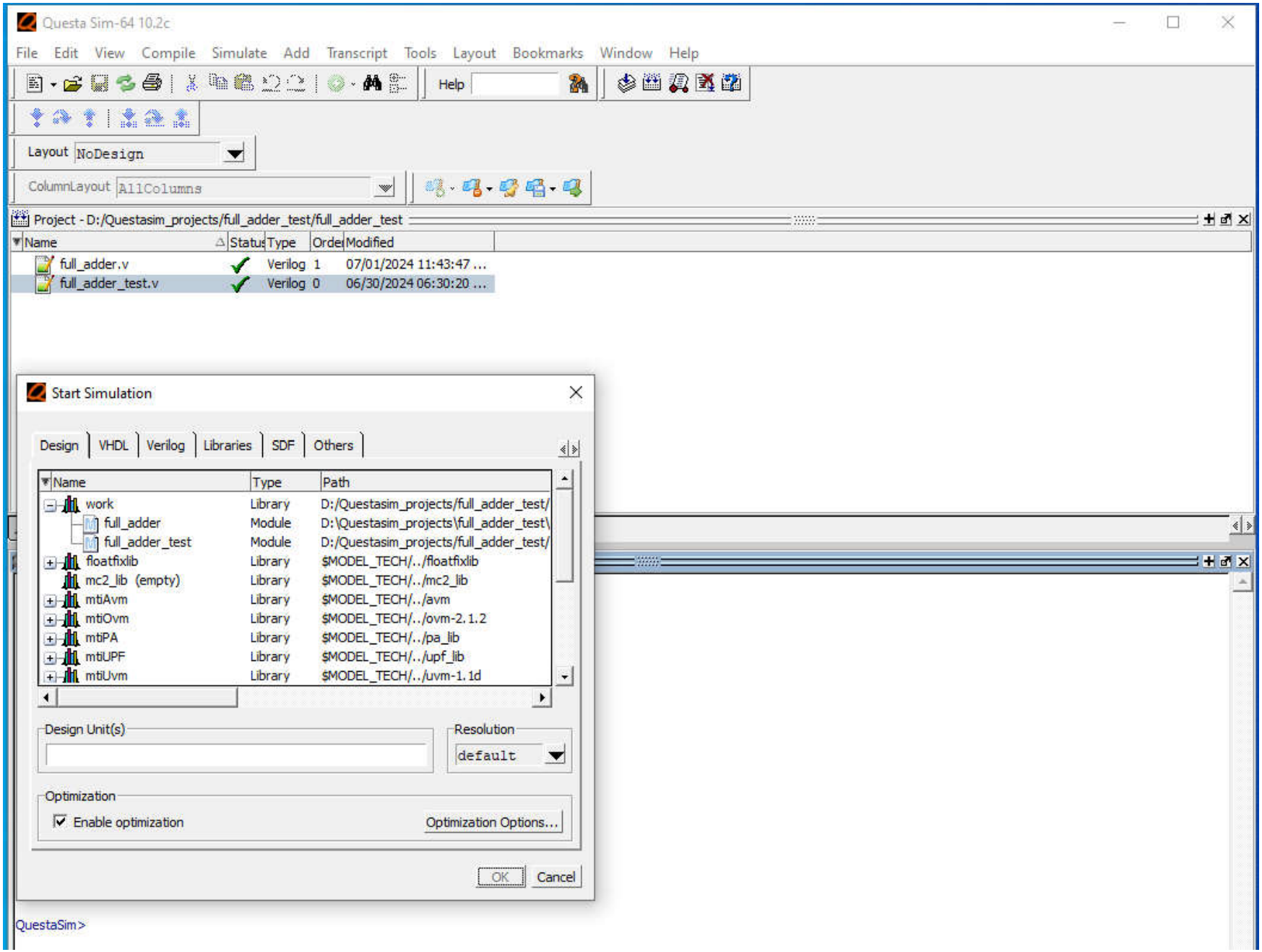
# Compile of full_adder_test.v was
QuestaSim>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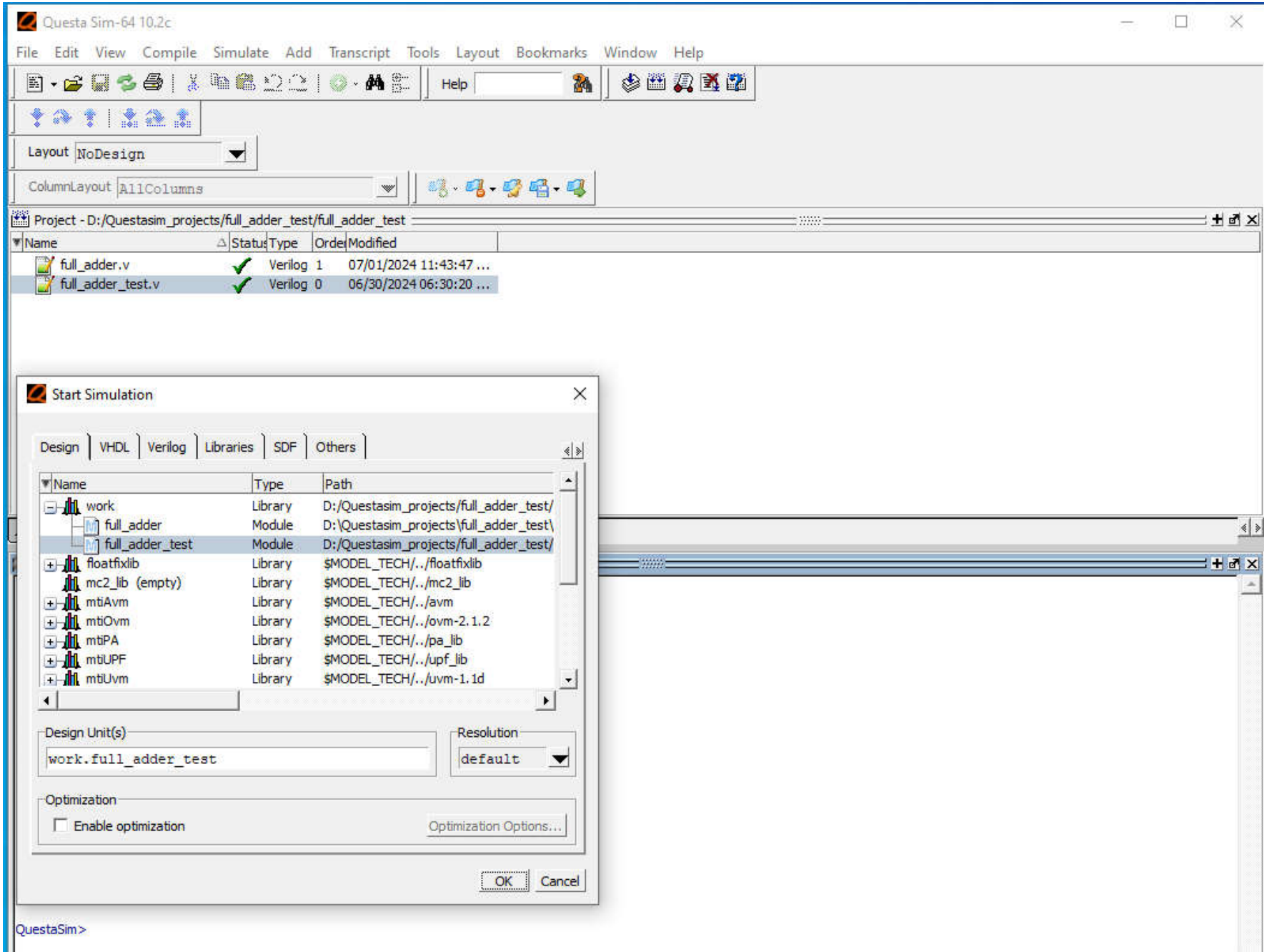
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
Help
Layout NoDesign
ColumnLayout AllColumns
Project - D:/Questasim_projects/full_adder_test/full_adder_test
Name Status Type Order Modified
full_adder.v Verilog 1 07/01/2024 11:43:47 ...
full_adder_test.v Verilog 0 06/30/2024 06:30:20 ...
Start Simulation
Design VHDL Verilog Libraries SDF Others
Name Type Path
work Library D:/Questasim_projects/full_adder_test/
full_adder Module D:\Questasim_projects\full_adder_test\
full_adder_test Module D:/Questasim_projects/full_adder_test/
floatfixlib Library $MODEL_TECH/../floatfixlib
mc2_lib (empty) Library $MODEL_TECH/../mc2_lib
mtiAvm Library $MODEL_TECH/../avm
mtiOvm Library $MODEL_TECH/../ovm-2.1.2
mtiPA Library $MODEL_TECH/../pa_lib
mtiUPF Library $MODEL_TECH/../upf_lib
mtiUvm Library $MODEL_TECH/../uvm-1.1d
Design Unit(s)
Resolution
default
Optimization
Enable optimization
Optimization Options...
OK
Cancel
QuestaSim>


Questa Sim-64 10.2c
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Layout NoDesign
ColumnLayout AllColumns
Project - D:/Questasim_projects/full_adder_test/full_adder_test
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full_adder.v Verilog 1 07/01/2024 11:43:47 ...
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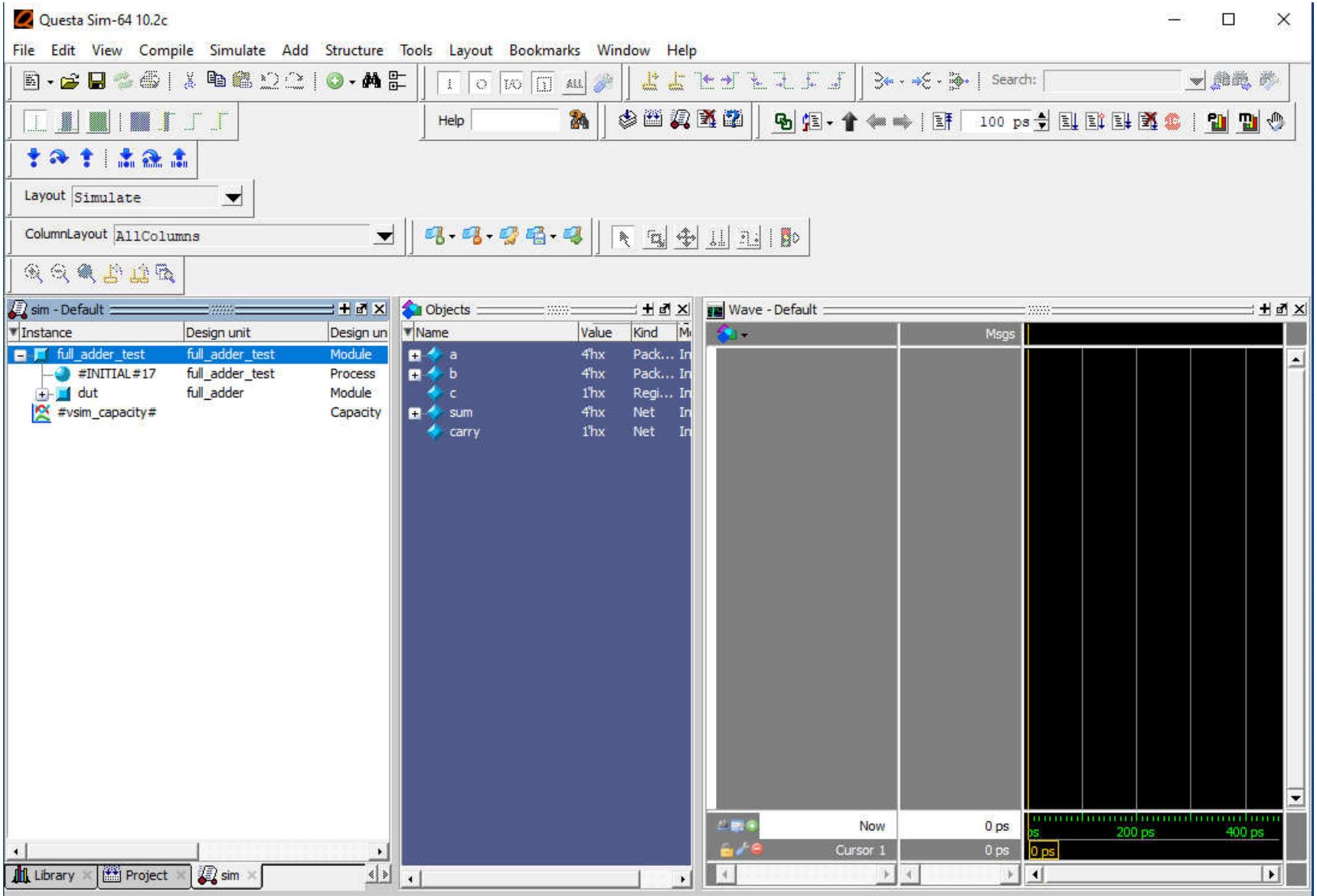
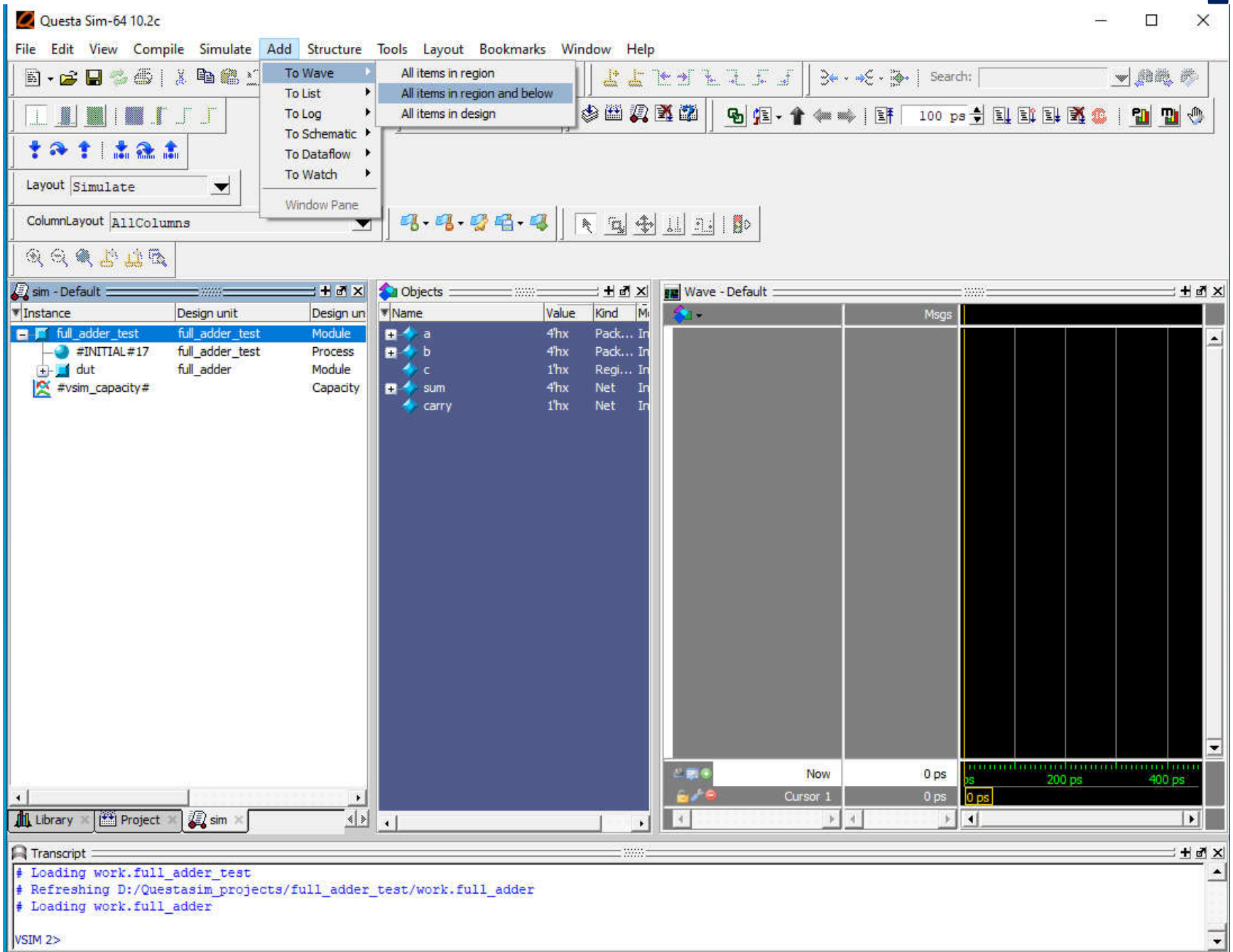
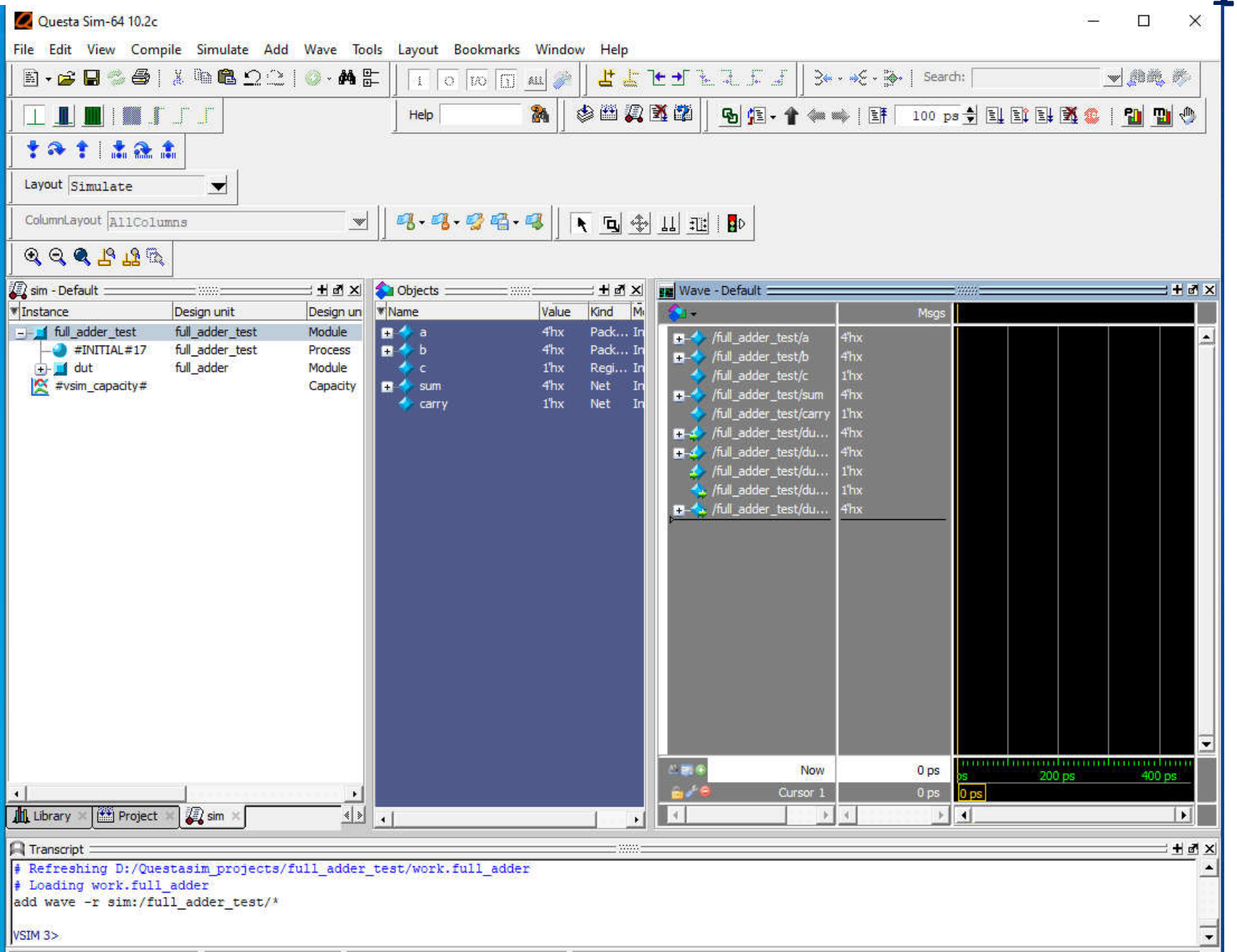
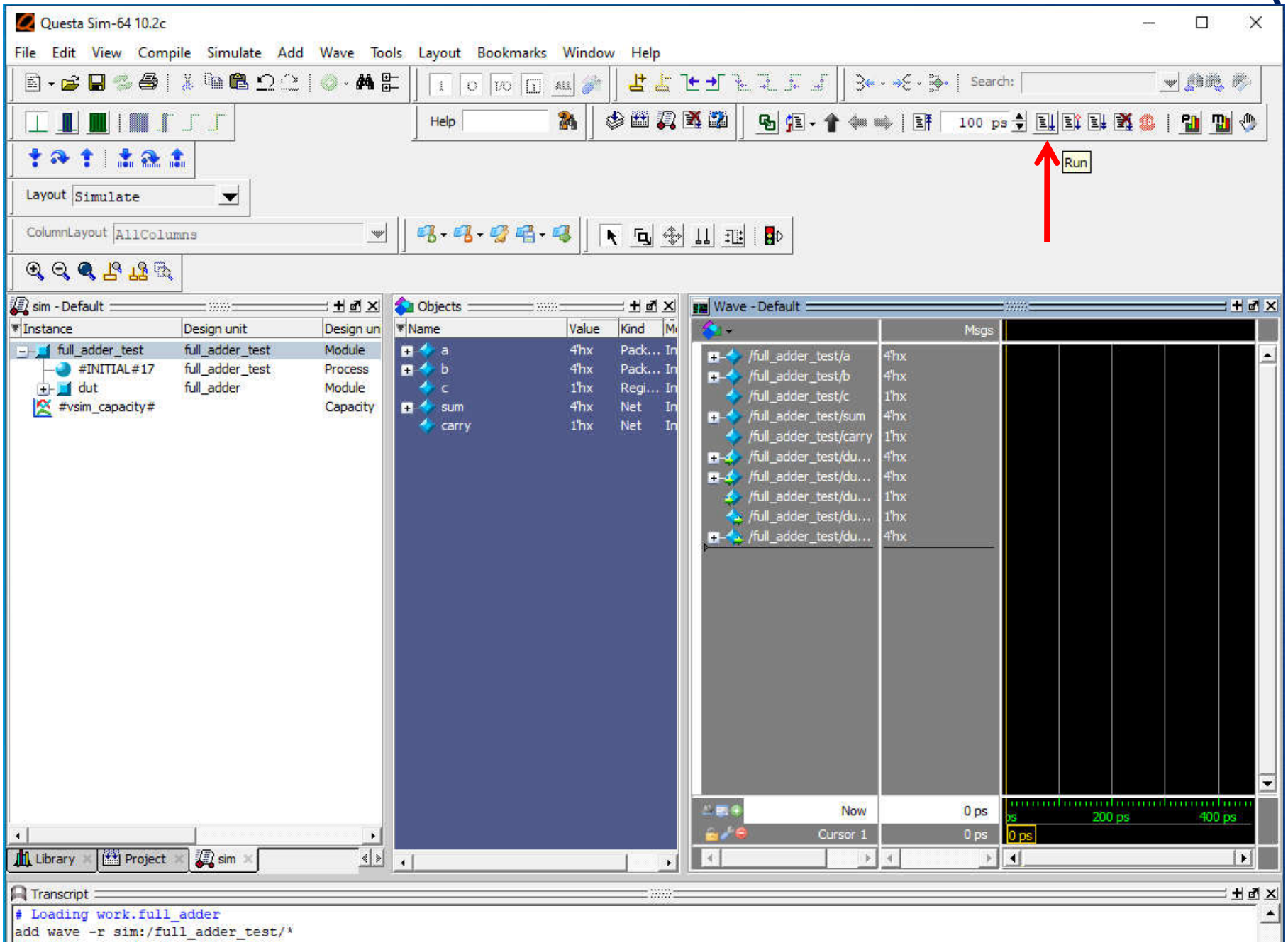
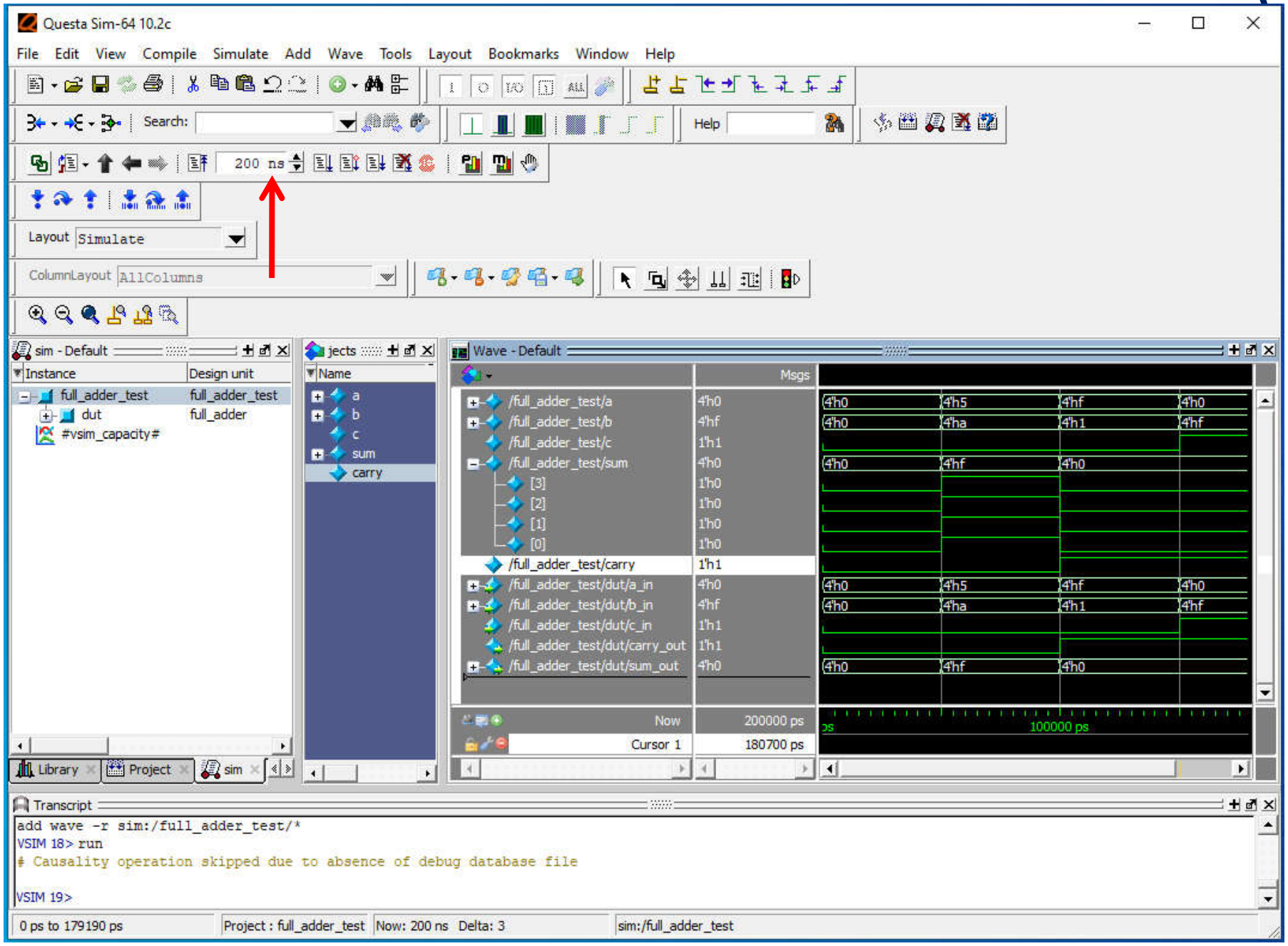
Design VHDL Verilog Libraries SDF Others
Name Type Path
work Library D:/Questasim_projects/full_adder_test/
full_adder Module D:\Questasim_projects\full_adder_test\
full_adder_test Module D:/Questasim_projects/full_adder_test/
floatfixlib Library $MODEL_TECH/../floatfixlib
mc2_lib (empty) Library $MODEL_TECH/../mc2_lib
mtiAvm Library $MODEL_TECH/../avm
mtiOvm Library $MODEL_TECH/../ovm-2.1.2
mtiPA Library $MODEL_TECH/../pa_lib
mtiUPF Library $MODEL_TECH/../upf_lib
mtiUvm Library $MODEL_TECH/../uvm-1.1d
Design Unit(s)
work.full_adder_test
Resolution
default
Optimization
Enable optimization
Optimization Options...
OK
Cancel
QuestaSim>

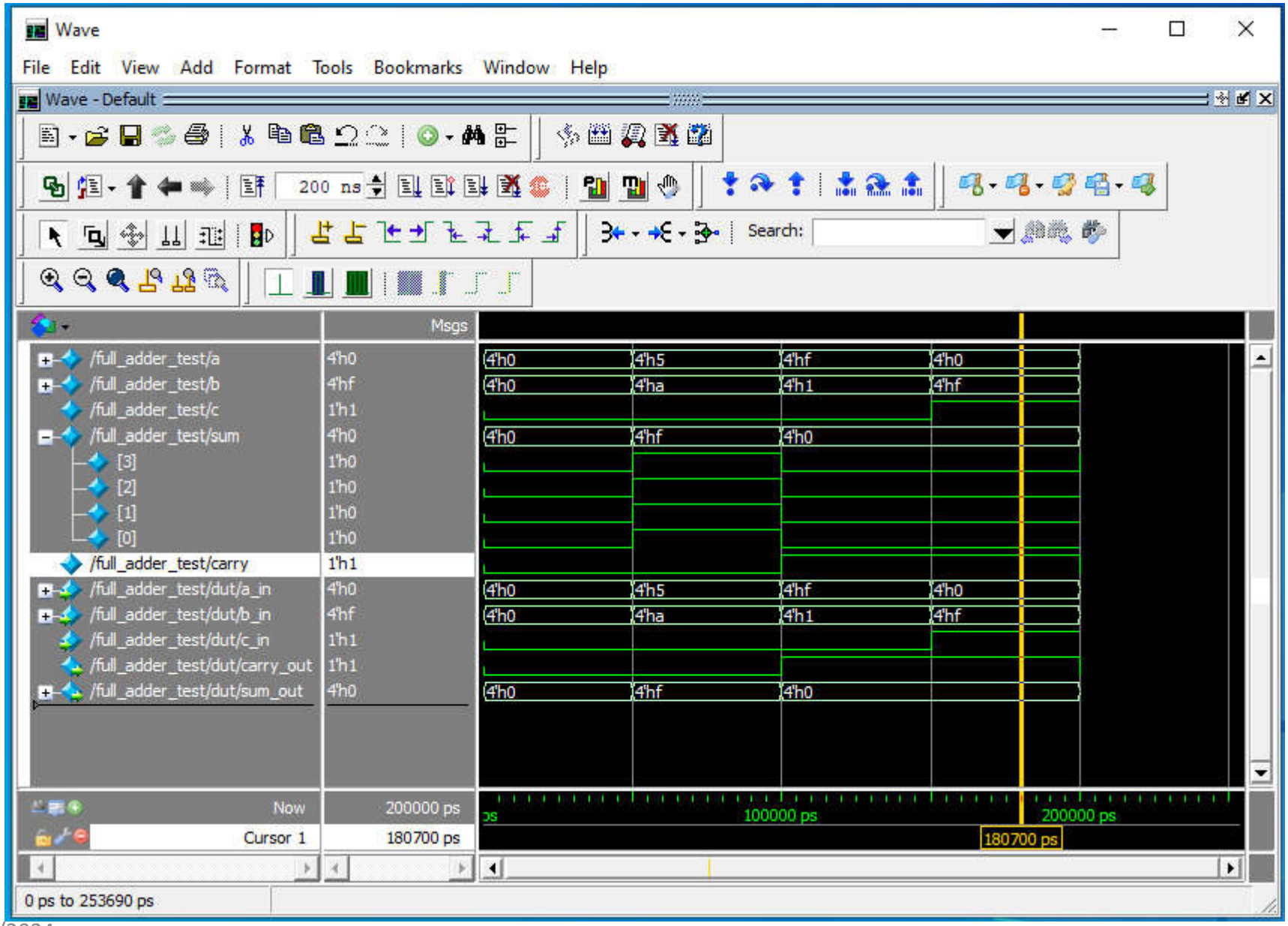

Questa Sim-64 10.2c
File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help
Search:
Help
100 ps
Layout Simulate
ColumnLayout AllColumns
sim - Default
Instance Design unit Design un
full_adder_test full_adder_test Module
#INITIAL#17 full_adder_test Process
dut full_adder Module
#vsim_capacity# Capacity
Objects
Name Value Kind
a 4'hx Pack... In
b 4'hx Pack... In
c 1'hx Regi... In
sum 4'hx Net In
carry 1'hx Net In
Wave - Default
Msgs
Now 0 ps
Cursor 1 0 ps
200 ps 400 ps
0 ps
Library Project sim
Transcript
# Loading work.full_adder_test
# Refreshing D:/Questasim_projects/full_adder_test/work.full_adder
# Loading work.full_adder
VSIM 2>


Questa Sim-64 10.2c
File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help
To Wave
To List
To Log
To Schematic
To Dataflow
To Watch
Window Pane
All items in region
All items in region and below
All items in design
Search:
100 ps
Layout Simulate
ColumnLayout AllColumns
sim - Default
Instance Design unit Design un
full_adder_test full_adder_test Module
#INITIAL#17 full_adder_test Process
dut full_adder Module
#vsim_capacity# Capacity
Objects
Name Value Kind
a 4'hx Pack... In
b 4'hx Pack... In
c 1'hx Regi... In
sum 4'hx Net In
carry 1'hx Net In
Wave - Default
Msgs
Now 0 ps
Cursor 1 0 ps
200 ps 400 ps
0 ps
Library Project sim
Transcript
# Loading work.full_adder_test
# Refreshing D:/Questasim_projects/full_adder_test/work.full_adder
# Loading work.full_adder
VSIM 2>


Questa Sim-64 10.2c
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Search:
Help
100 ps
Layout Simulate
ColumnLayout AllColumns
sim - Default
Instance Design unit Design un
full_adder_test full_adder_test Module
#INITIAL#17 full_adder_test Process
dut full_adder Module
#vsim_capacity# Capacity
Objects
Name Value Kind
a 4'hx Pack...
b 4'hx Pack...
c 1'hx Regi...
sum 4'hx Net
carry 1'hx Net
Wave - Default
Msgs
/full_adder_test/a 4'hx
/full_adder_test/b 4'hx
/full_adder_test/c 1'hx
/full_adder_test/sum 4'hx
/full_adder_test/carry 1'hx
Now 0 ps
Cursor 1 0 ps
200 ps 400 ps
Library Project sim
Transcript
# Refreshing D:/Questasim_projects/full_adder_test/work.full_adder
# Loading work.full_adder
add wave -r sim:/full_adder_test/*
VSIM 3>


Questa Sim-64 10.2c
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Search:
Help
100 ps
Run
Layout Simulate
ColumnLayout AllColumns
sim - Default
Instance Design unit Design un
full_adder_test full_adder_test Module
#INITIAL#17 full_adder_test Process
dut full_adder Module
#vsim_capacity# Capacity
Objects
Name Value Kind
a 4'hx Pack... In
b 4'hx Pack... In
c 1'hx Regi... In
sum 4'hx Net In
carry 1'hx Net In
Wave - Default
Msgs
/full_adder_test/a 4'hx
/full_adder_test/b 4'hx
/full_adder_test/c 1'hx
/full_adder_test/sum 4'hx
/full_adder_test/carry 1'hx
Now 0 ps
Cursor 1 0 ps
200 ps 400 ps
Library Project sim
Transcript
# Loading work.full_adder
add wave -r sim:/full_adder_test/*


Questa Sim-64 10.2c
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Search:
Help
200 ns
Layout Simulate
ColumnLayout AllColumns
sim - Default
Instance
Design unit
full_adder_test
full_adder_test
dut
full_adder
#vsim_capacity#
jects
Name
a
b
c
sum
carry
Wave - Default
Msgs
/full_adder_test/a
/full_adder_test/b
/full_adder_test/c
/full_adder_test/sum
[3]
[2]
[1]
[0]
/full_adder_test/carry
/full_adder_test/dut/a_in
/full_adder_test/dut/b_in
/full_adder_test/dut/c_in
/full_adder_test/dut/carry_out
/full_adder_test/dut/sum_out
4'h0
4'hf
1'h1
4'h5
4'ha
4'h1
Now
200000 ps
Cursor 1
180700 ps
100000 ps
Library
Project
sim
Transcript
add wave -r sim:/full_adder_test/*
VSIM 18> run
# Causality operation skipped due to absence of debug database file
VSIM 19>
0 ps to 179190 ps
Project : full_adder_test
Now: 200 ns Delta: 3
sim:/full_adder_test


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
200 ns
Search:
Msgs
/full_adder_test/a 4'h0
/full_adder_test/b 4'hf
/full_adder_test/c 1'h1
/full_adder_test/sum 4'h0
[3] 1'h0
[2] 1'h0
[1] 1'h0
[0] 1'h0
/full_adder_test/carry 1'h1
/full_adder_test/dut/a_in 4'h0
/full_adder_test/dut/b_in 4'hf
/full_adder_test/dut/c_in 1'h1
/full_adder_test/dut/carry_out 1'h1
/full_adder_test/dut/sum_out 4'h0
4'h0 4'h5 4'hf 4'h0
4'h0 4'ha 4'h1 4'hf
4'h0 4'hf 4'h0
4'h0 4'h5 4'hf 4'h0
4'h0 4'ha 4'h1 4'hf
4'h0 4'hf 4'h0
Now 200000 ps
Cursor 1 180700 ps
100000 ps
200000 ps
180700 ps
0 ps to 253690 ps

# Thank You