Questasim Tutorial (GUI/Windows)

REF: ELEC 5200/6200, Spring 2009, Modelsim Tutorial

Step 0

- Create a directory for DUT and Test Bench files.
 - E.g.,
 - D:\Questasim_projects\full_adder_test
- Write your Verilog HDL code in a text editor (e.g., notepad++)
- Save file as .v files in the directory created above.

PC > Local Disk (D:) > Questasim	Search full_adder_test		
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🎽 full_adder_test.v	6/30/2024 6:30 PM	V File	1 KB

To simulate using Questasim, follow the steps on the Next Slides.

• Start Questasim by double clicking on the icon:



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• After starting the Questasim,

- Create a **New / Project** from the **File** menu as shown in Figure below.

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• Give Project Name a name. [full_adder_test]

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- After clicking OK, a window, as shown below, will pop up. ٠
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- Make sure that you select "Copy to Project Directory" option. Click OK.

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- Make sure that you select "Copy to Project Directory" option. Click OK.

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• The selected Verilog files will appear in the workspace (**Project** window).



• Select Verilog file, then click the compile icon at the top as highlighted by red arrow in the figure below and the design will be compiled.

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Select Verilog file, then click the Compile menu at the top as shown in the figure below, choose Compile Selected and the design will be compiled.
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• If errors happen to the design, the tool shows info colored w/ RED line.

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• Select **Compile Report** to see errors.

• Select **Compile Report** to see errors.

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Note: Double click the error message and a **window** will appear which will contain description of the error and the line no. on which the error has occurred.

11 (2)

• Select **Compile Report** to see errors.

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module full_adder (a_in, b_in, c_in, c_out, sum_out);
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      input [3:0] a in, b in;
 5
 6
     input c in;
 7
     output carry out;
 8
      output [3:0] sum out;
 9
10
     reg carry out;
     reg [3:0] sum_out;
11
12
13
      always @ (a in or b in or c in)
14
          begin
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15
               {carry out, sum out} = a in + b in + c in;
16
          end
17
18
      endmodule
```

11 (3)

11 (4)

```
module full_adder (a_in, b_in, c_in, carry_out, sum_out);
 3
 4
 5
     input [3:0] a in, b in;
 6
     input c in;
 7
     output carry out;
     output [3:0] sum_out;
 8
 9
10
     reg carry out;
11
     reg [3:0] sum out;
12
13
     always @ (a in or b in or c in)
14
         begin
    15
              {carry out, sum out} = a in + b in + c in;
16
         end
17
18
     endmodule
```

11 (5)

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• Double click on **full_adder_test.v** file, choose **Compile Selected** to run...

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After compilation is successful,

• we **simulate** the design using an icon highlighted by **RED** arrow in figure.

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