ASIC/FPGA Design and Verification

Part 2: Typical EDA Tool

Tuan Nguyen-viet

Vivado

- AMD/Xilinx Vivado is an advanced suite for digital logic design and FPGA based implementation to
  - develop,
  - simulate,
  - synthesize,
  - implement
    - RTL designs on AMD/Xilinx FPGA device.

Installing

- Sign up for a AMD/Xilinx account to download Vivado running on Windows.

- Choose the FPGA family to work with: e.g., Artix, Zynq, etc.

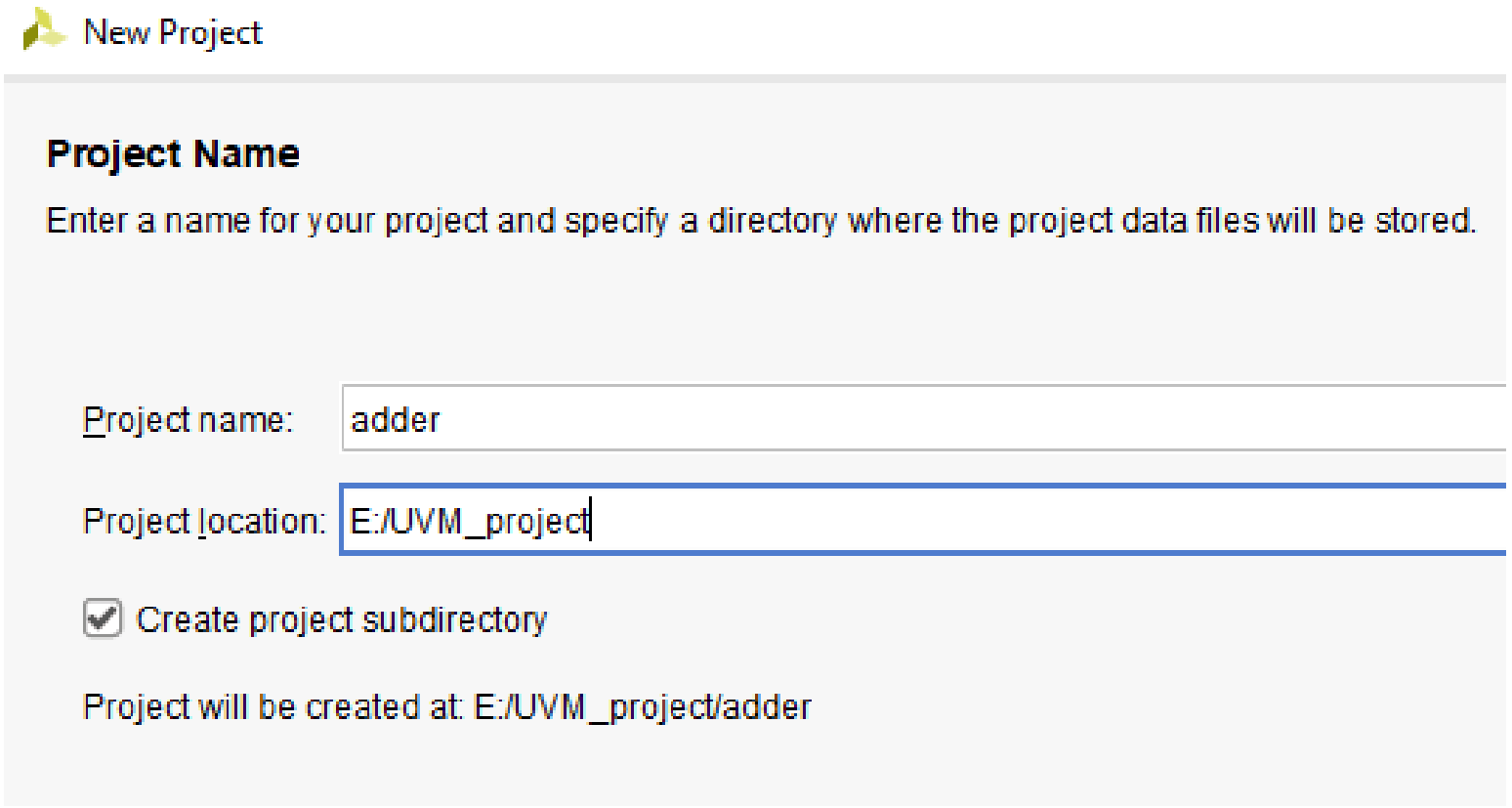
GUI

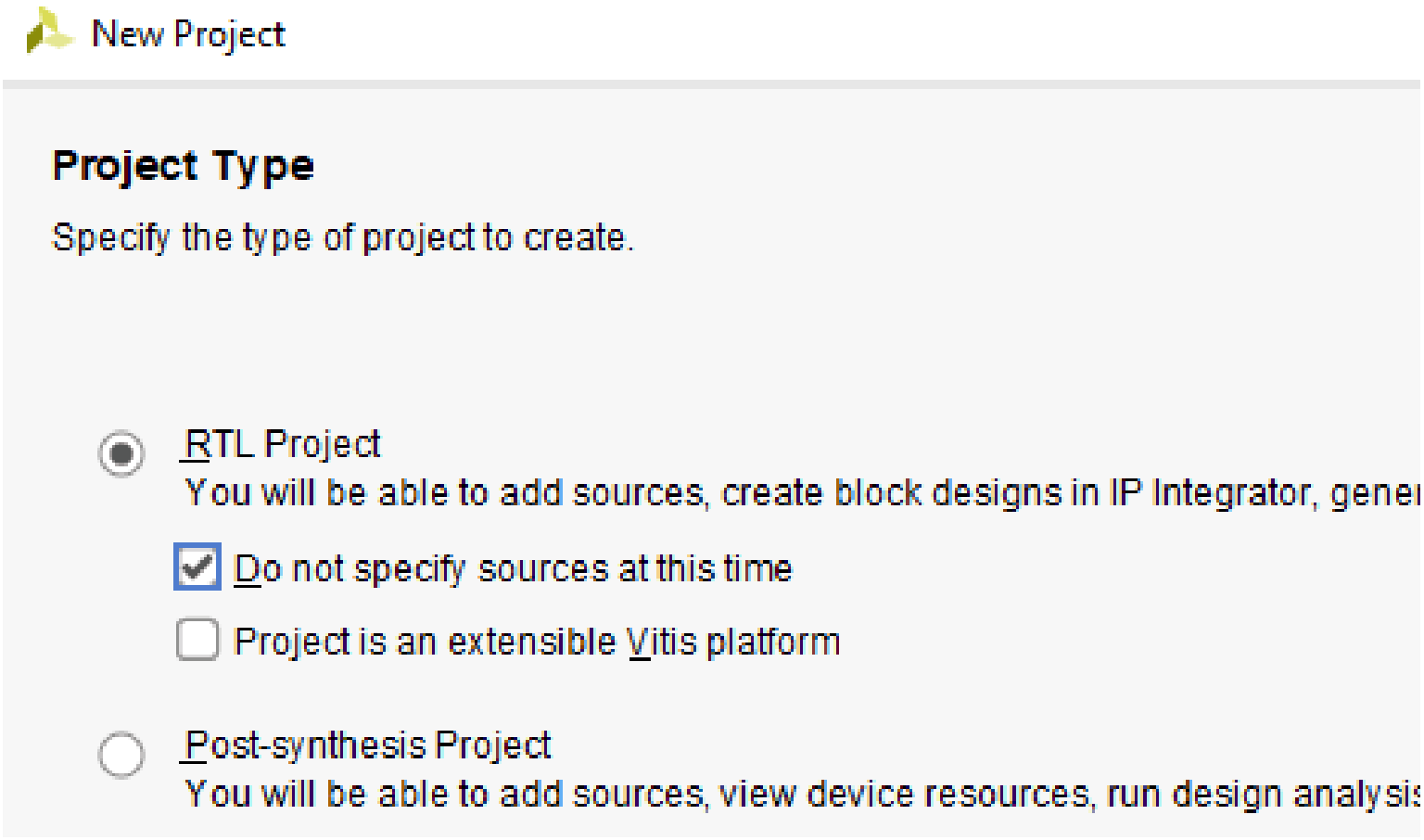
Creating an RTL Design Project

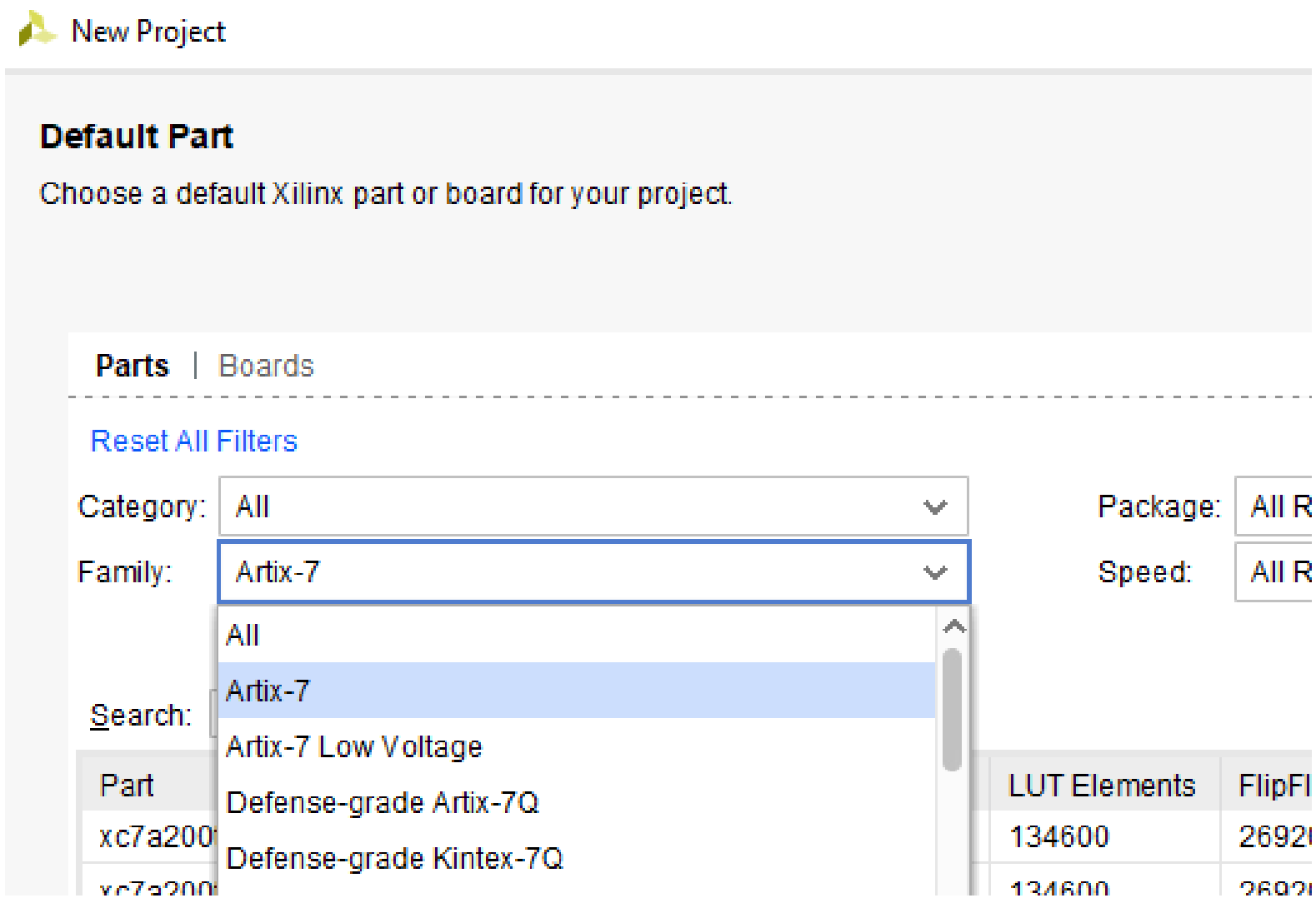
- Launch Vivado from the desktop

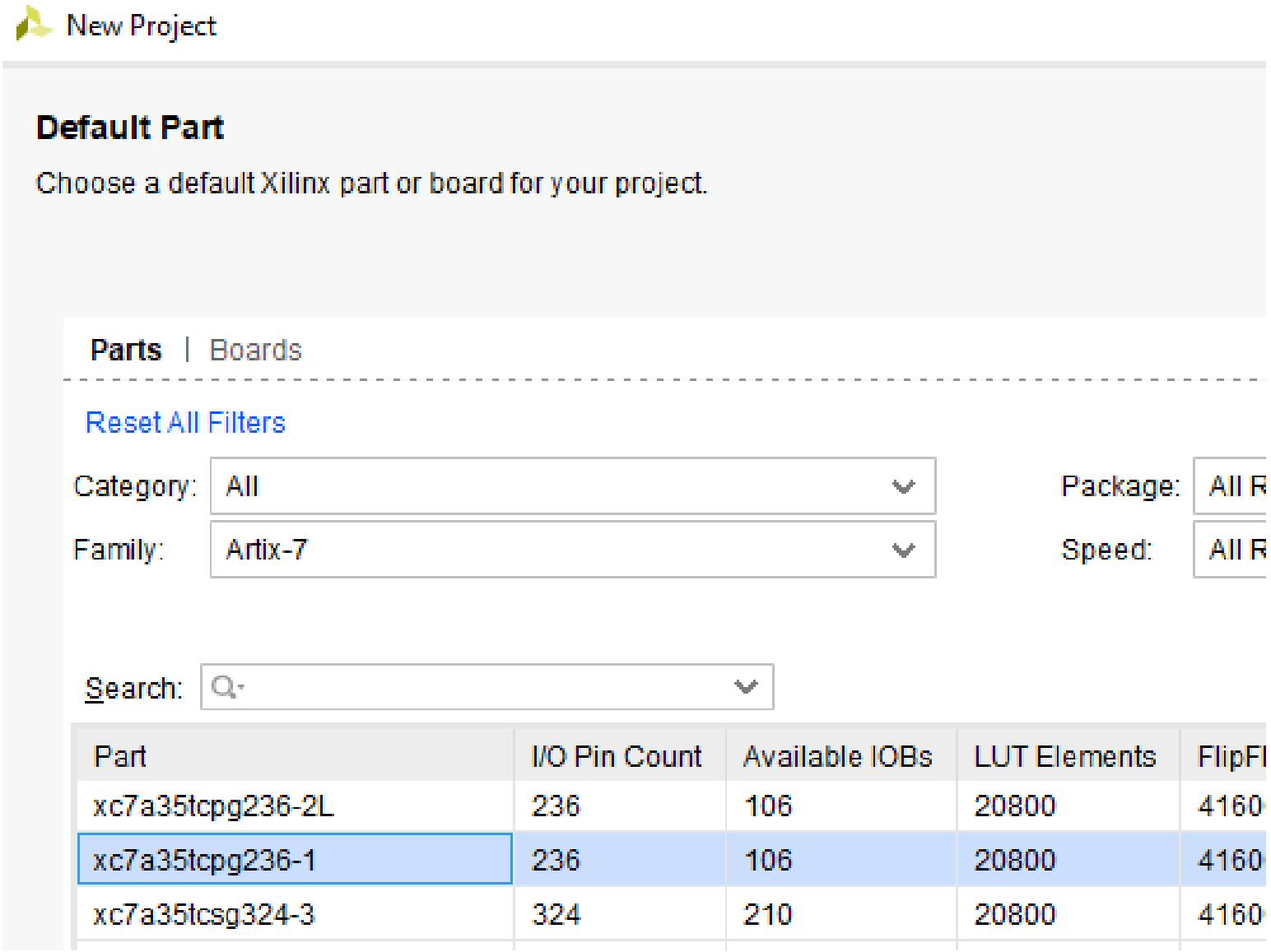
- Create a New Project:
  - Click on **Create Project**
  - Choose a project name and location.
  - Select **RTL Project**
    - and ensure **Do Not specify sources at this time** is checked.
  - Choose the target FPGA device.
    - e.g., using an Artix-7,
      - select the corresponding part number (e.g., **xc7a35tcpg236–1**).

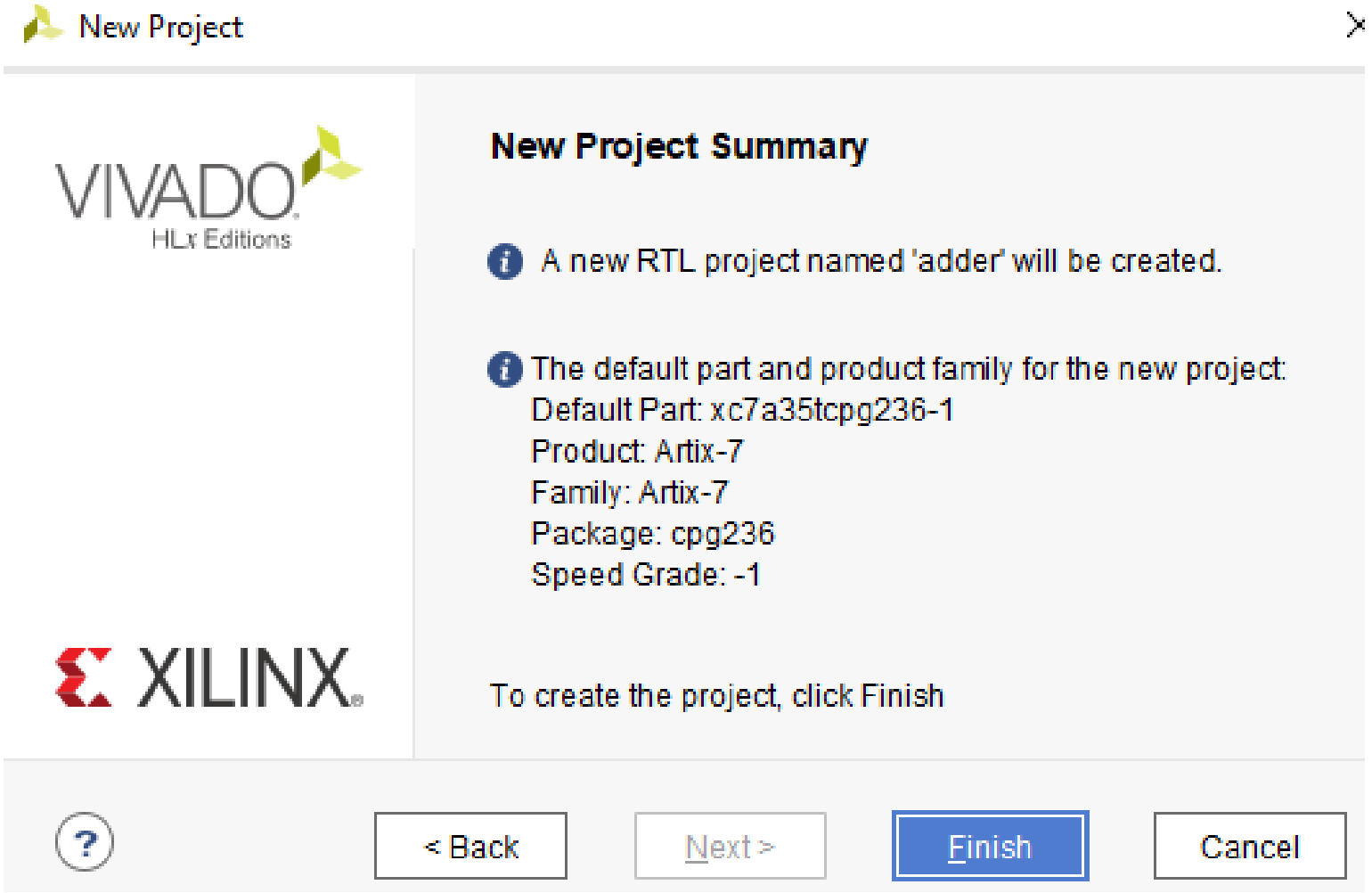

VIVADO
HLx Editions
Quick Start
Create Project
Open Project
Open Example Project

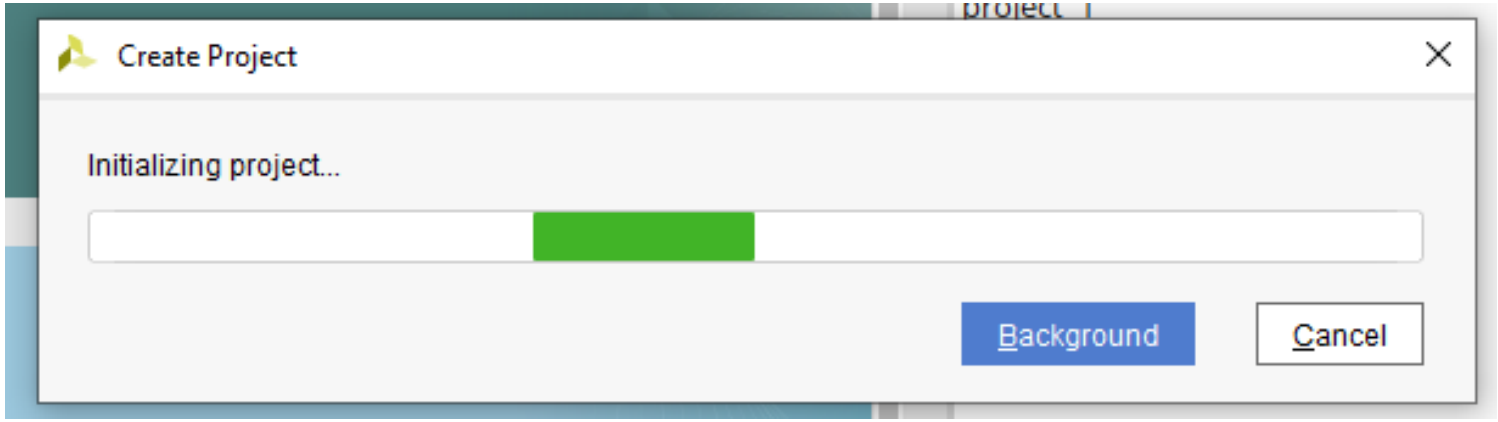

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
adder
Project location:
E:/UVM_project
Create project subdirectory
Project will be created at: E:/UVM_project/adder


New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, gener
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis


New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Category: All
Family: Artix-7
Package: All R
Speed: All R
All
Artix-7
Artix-7 Low Voltage
Defense-grade Artix-7Q
Defense-grade Kintex-7Q
Search:
Part
LUT Elements
FlipFl
xc7a200
134600
2692


New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Category: All
Family: Artix-7
Package: All R
Speed: All R
Search:
Part
I/O Pin Count
Available IOBs
LUT Elements
FlipFl
xc7a35tcpg236-2L
236
106
20800
4160
xc7a35tcpg236-1
236
106
20800
4160
xc7a35tcsg324-3
324
210
20800
4160

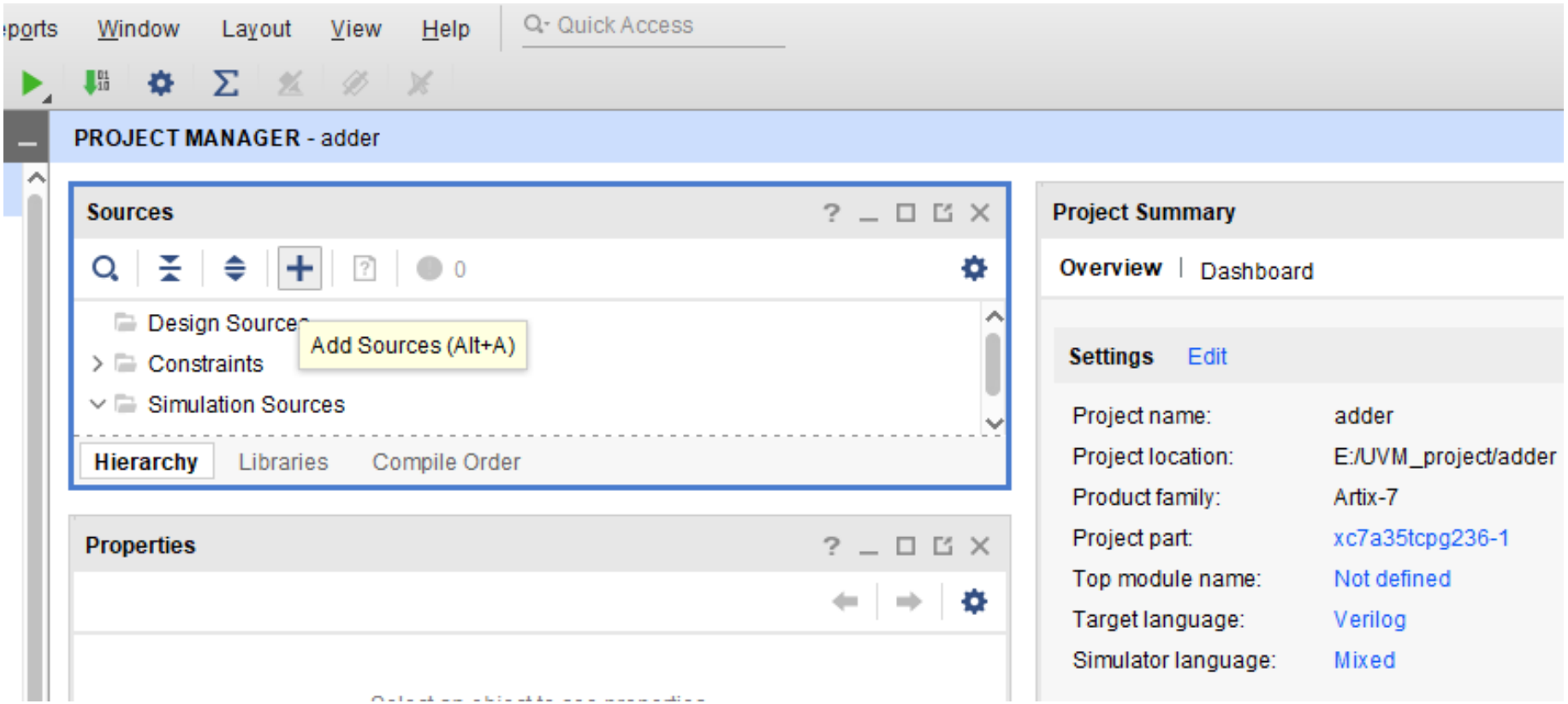

New Project
VIVADO
HLx Editions
New Project Summary
A new RTL project named 'adder' will be created.
The default part and product family for the new project:
Default Part: xc7a35tcpg236-1
Product: Artix-7
Family: Artix-7
Package: cpg236
Speed Grade: -1
XILINX
To create the project, click Finish
< Back
Next >
Finish
Cancel

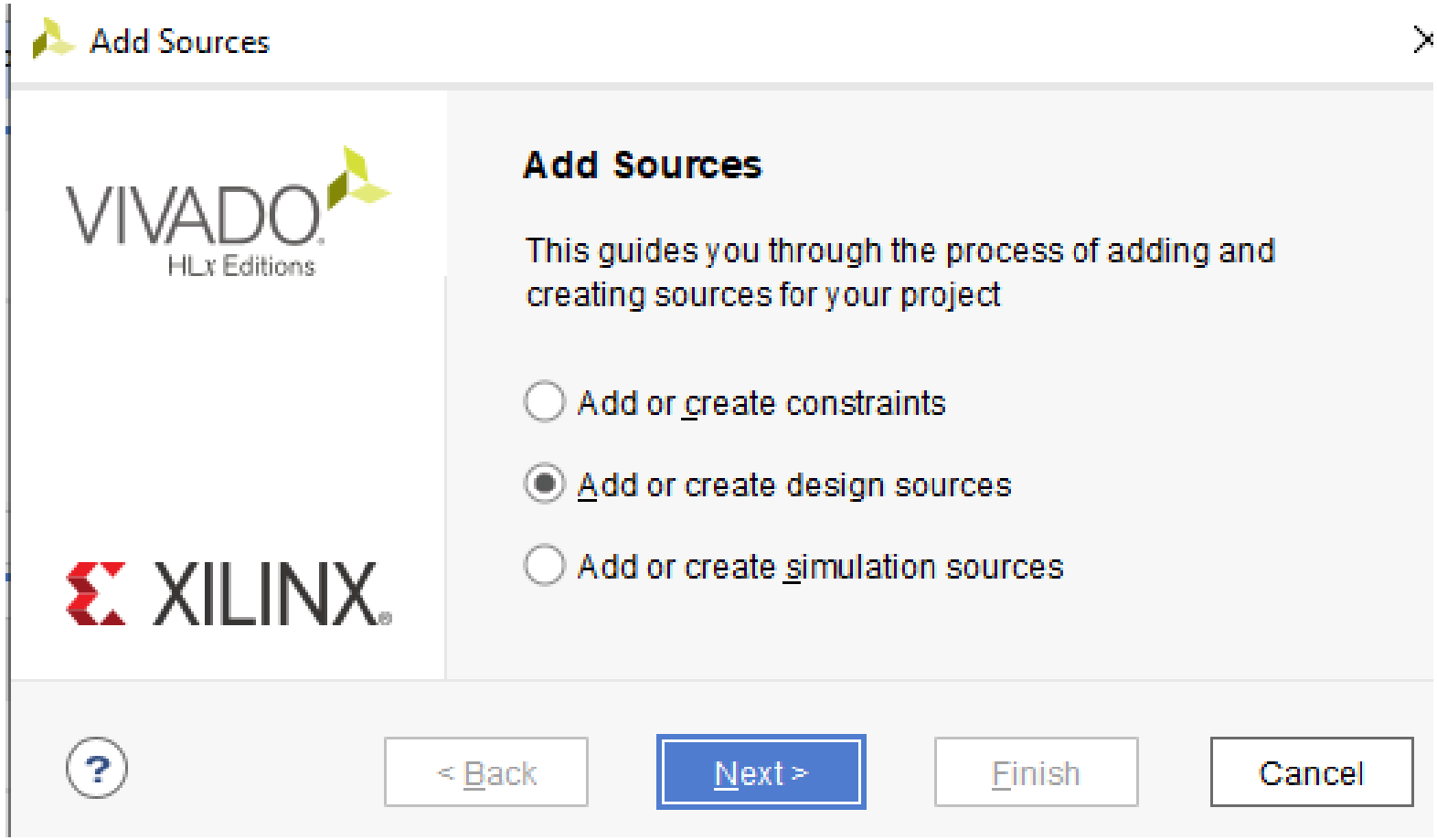

Create Project
Initializing project...
Background
Cancel

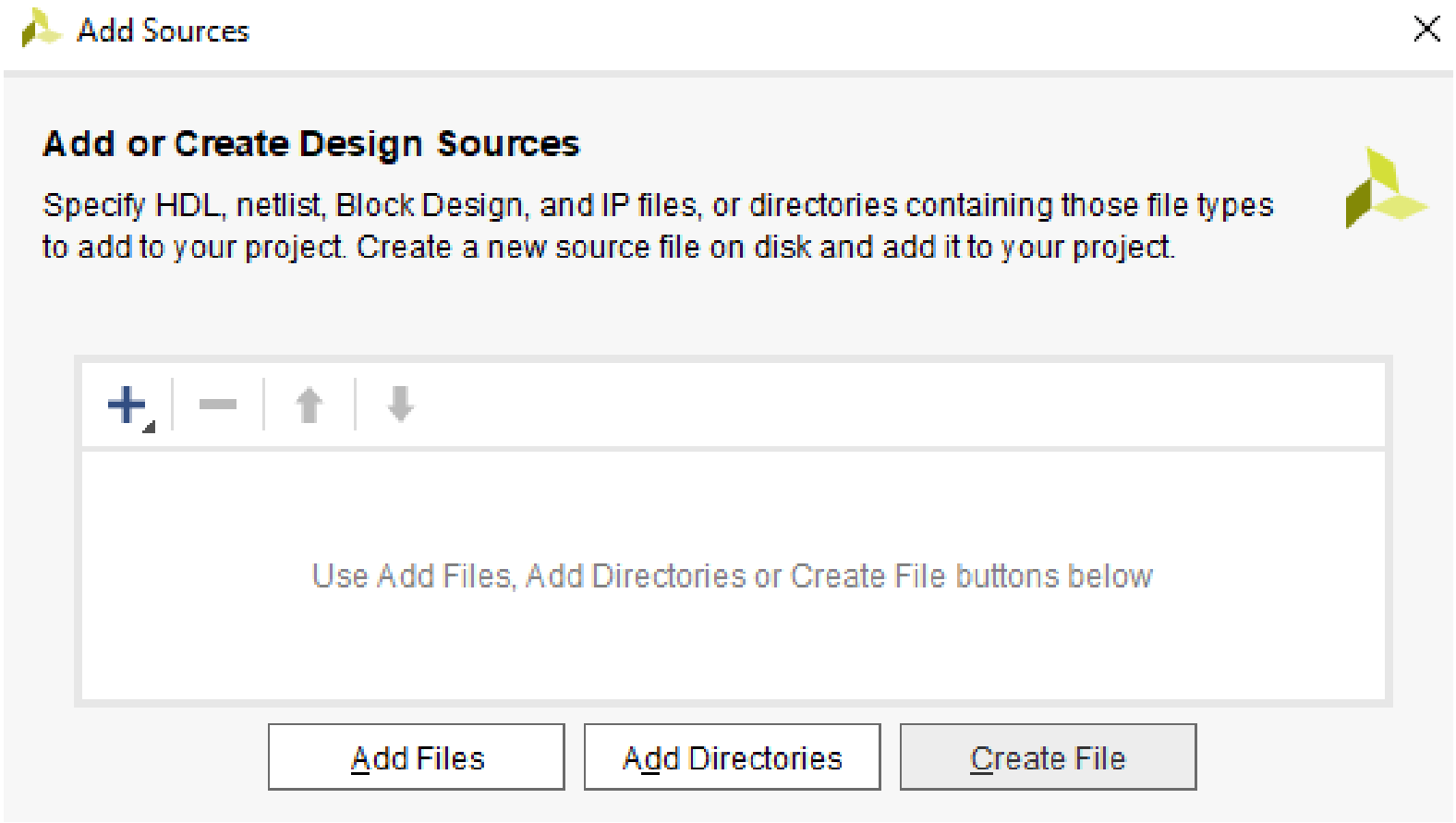
Creating/Adding an RTL Design

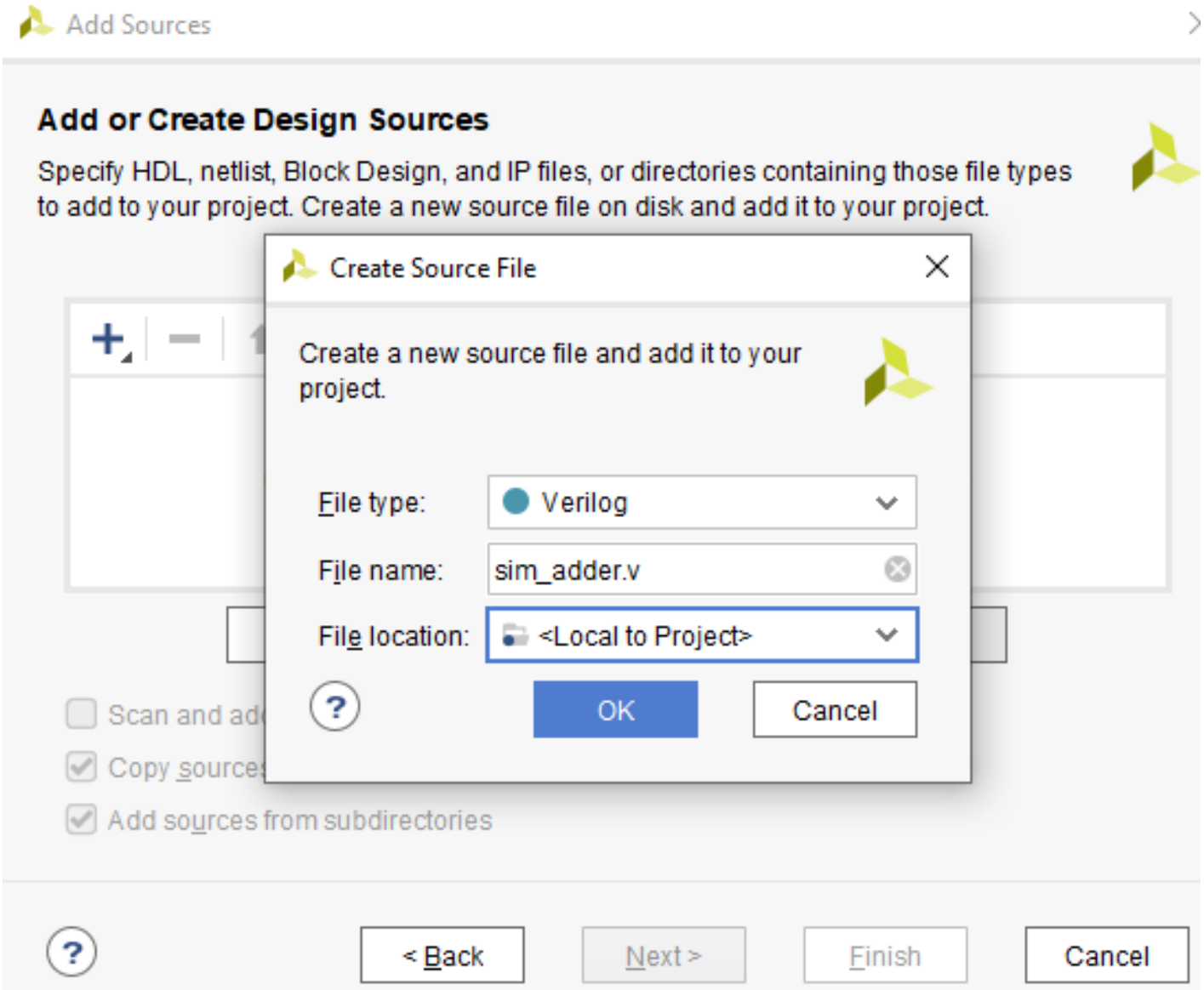
- Add RTL Design
  - In the **Project Manager**, click **Add Sources**.
  - Select **Add or Create Design Sources**, then click **Next**.
    - Click **Create File**, select **Verilog** as the file type, name it **sim_adder.v**, and click **OK**.
  - **Finish** adding the file to the project.

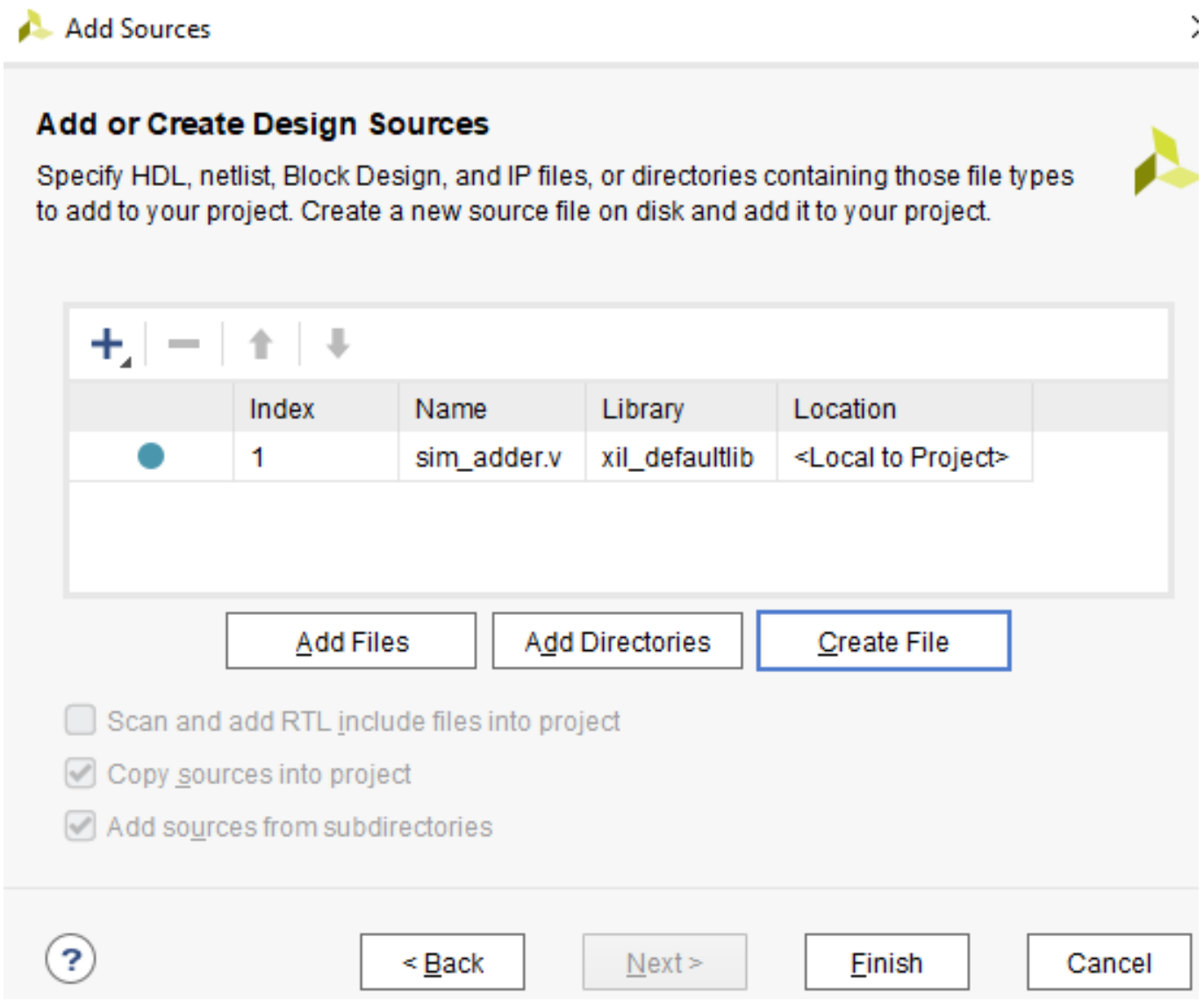
- Open the newly created **sim_adder.v** file and add the Verilog code for a simple 2-bit adder.

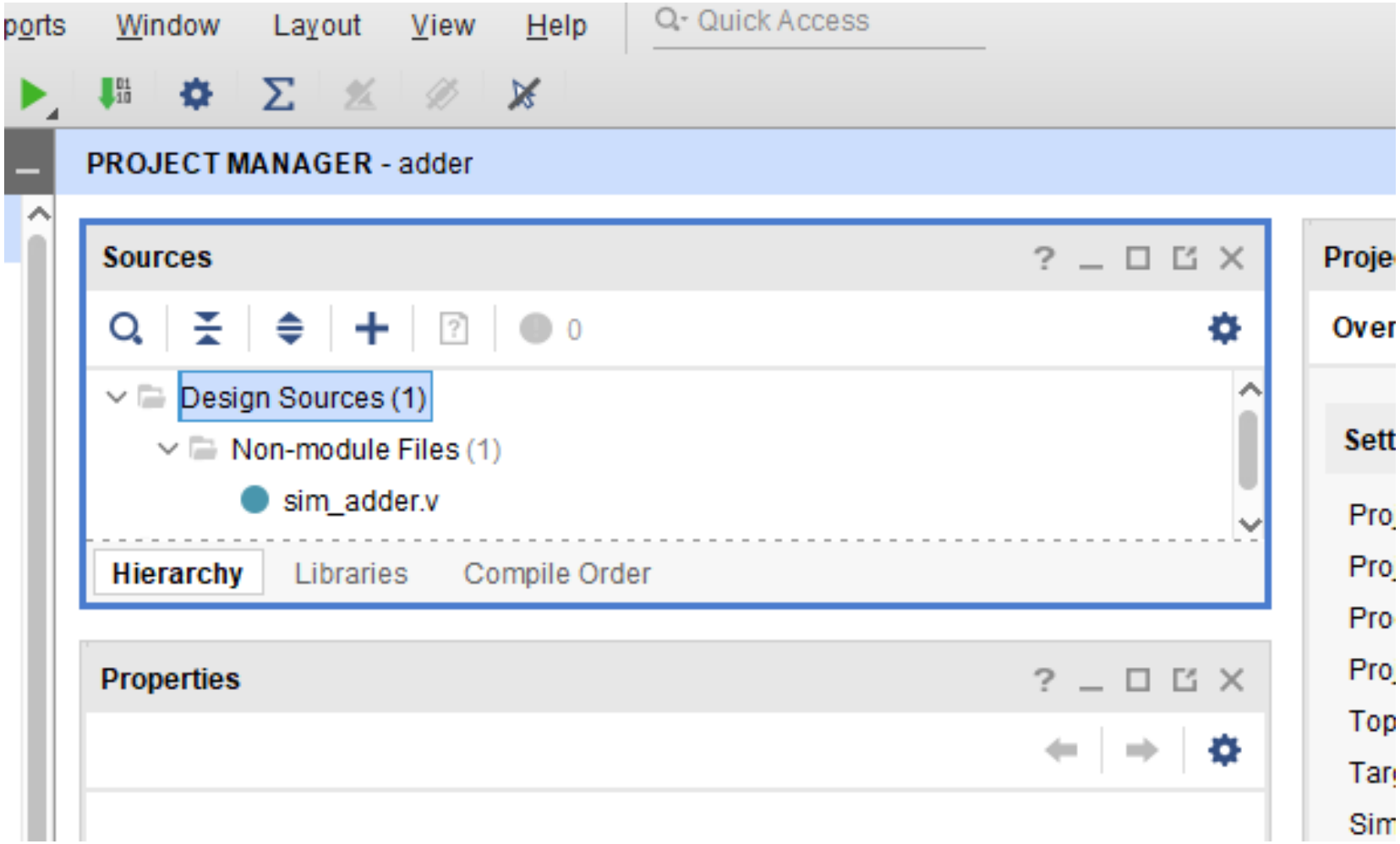

Window
Layout
View
Help
Quick Access
PROJECT MANAGER - adder
Sources
Design Sources
Add Sources (Alt+A)
Constraints
Simulation Sources
Hierarchy
Libraries
Compile Order
Properties
Project Summary
Overview
Dashboard
Settings
Edit
Project name: adder
Project location: E:/UVM_project/adder
Product family: Artix-7
Project part: xc7a35tcpg236-1
Top module name: Not defined
Target language: Verilog
Simulator language: Mixed


Add Sources
VIVADO
HLx Editions
XILINX
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File


Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Create Source File
Create a new source file and add it to your project.
File type:
Verilog
File name:
sim_adder.v
File location:
<Local to Project>
OK
Cancel
Scan and ad
Copy sources
Add sources from subdirectories
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Index
Name
Library
Location
1
sim_adder.v
xil_defaultlib
<Local to Project>
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel


ports
Window
Layout
View
Help
Quick Access
PROJECT MANAGER - adder
Sources
0
Design Sources (1)
Non-module Files (1)
sim_adder.v
Hierarchy
Libraries
Compile Order
Properties
Proje
Over
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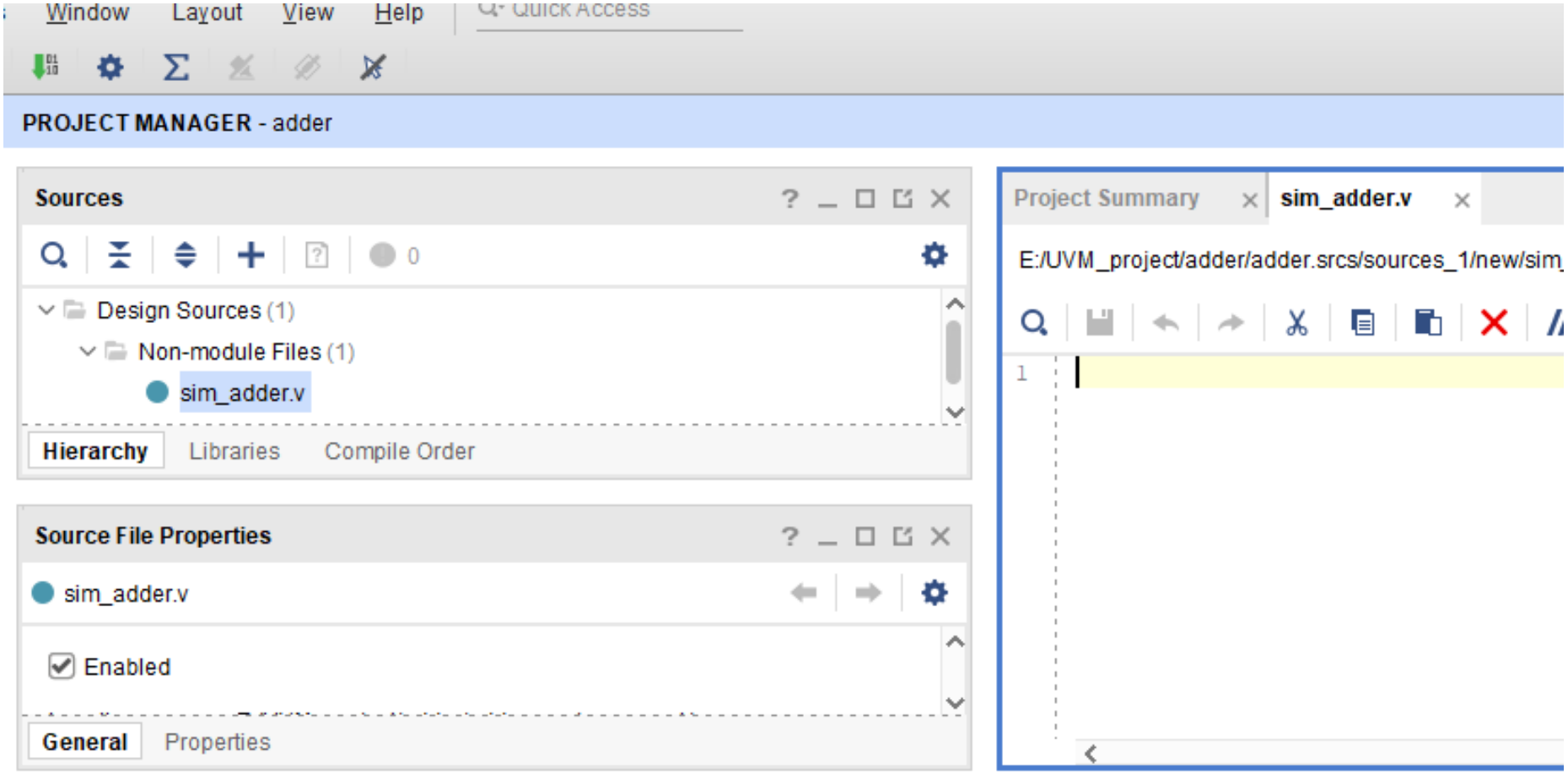
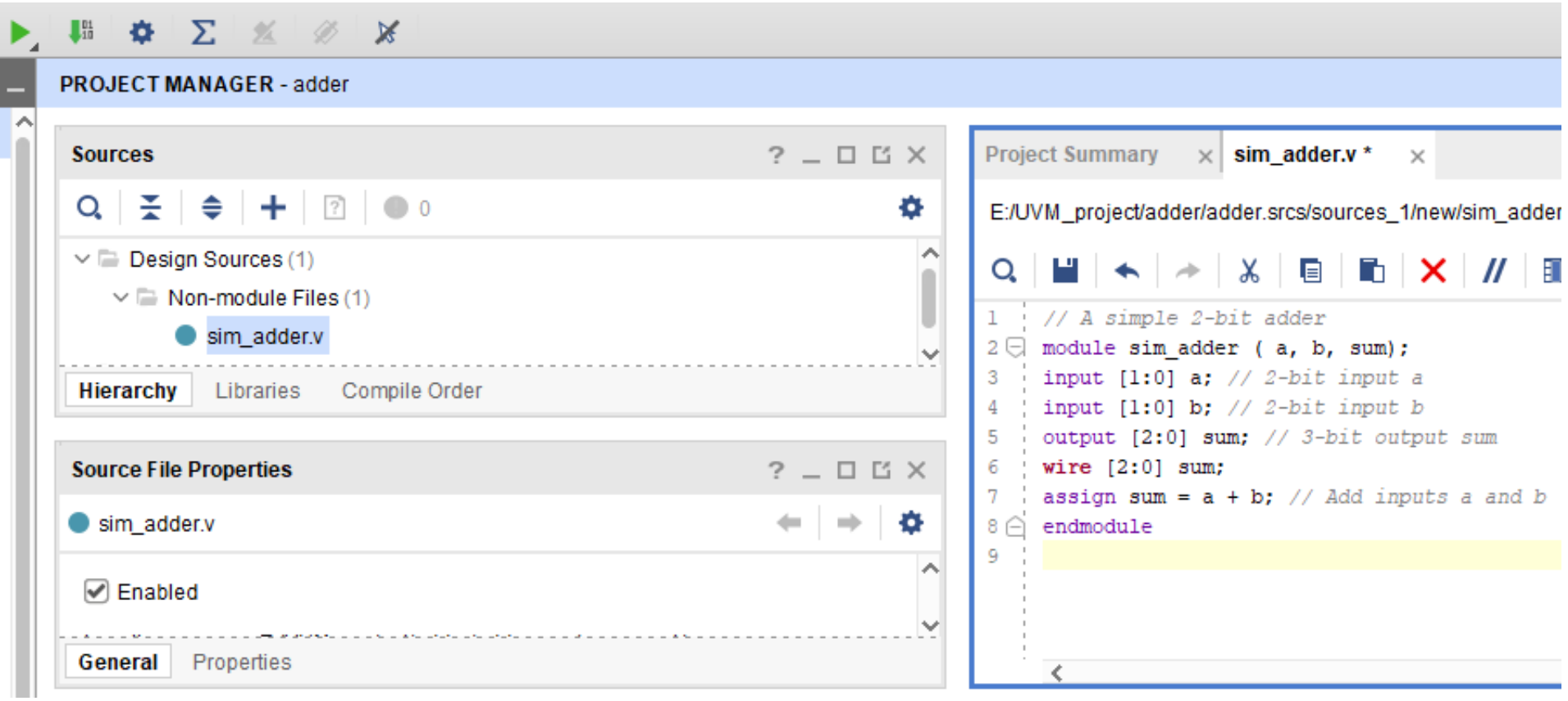

Window
Layout
View
Help
Quick Access
PROJECT MANAGER - adder
Sources
0
Design Sources (1)
Non-module Files (1)
sim_adder.v
Hierarchy
Libraries
Compile Order
Source File Properties
sim_adder.v
Enabled
General
Properties
Project Summary
sim_adder.v
E:/UVM_project/adder/adder.srcs/sources_1/new/sim
1

Creating/Adding an RTL Design (2)

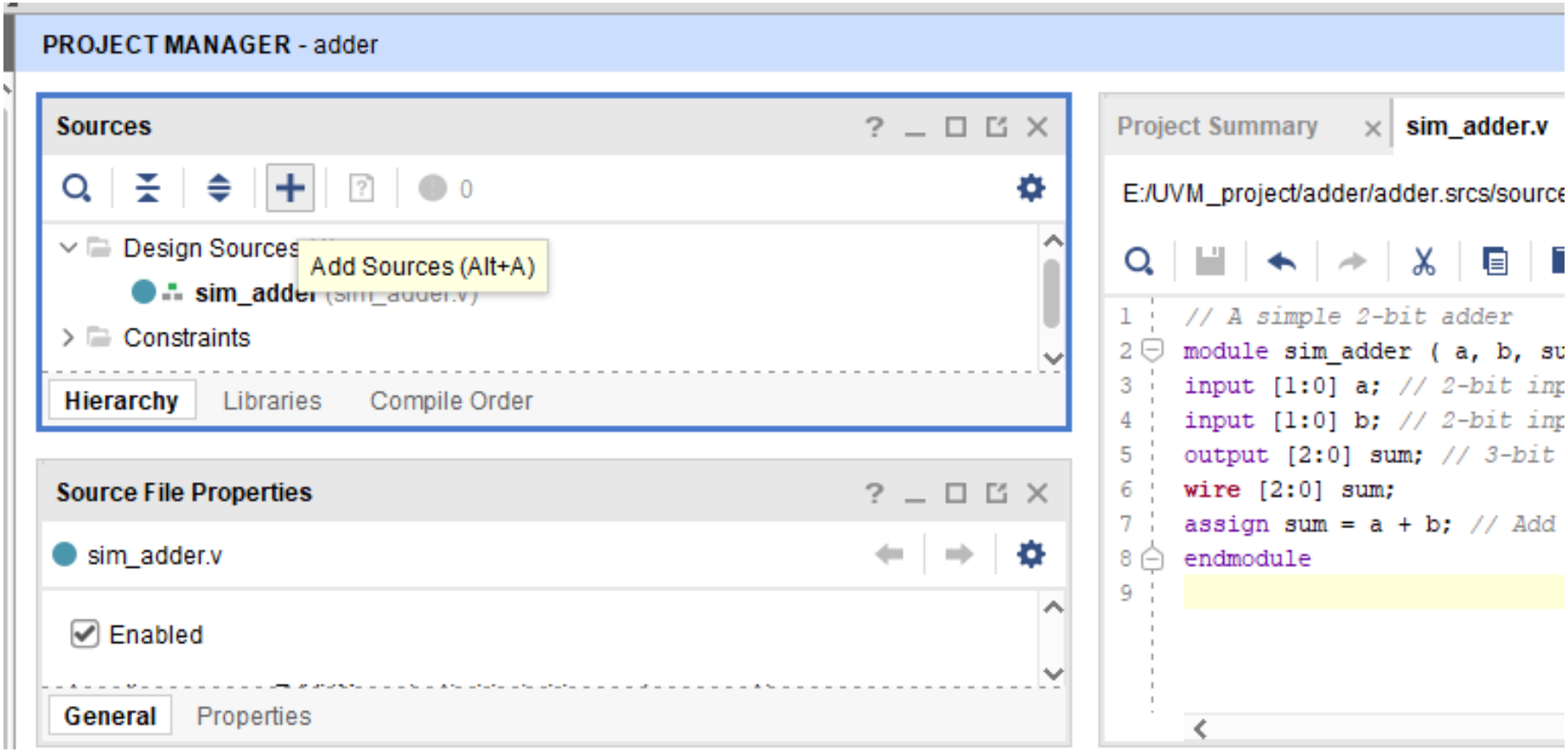
```
// A simple 2-bit adder
module sim_adder ( a, b, sum);
input [1:0] a; // 2-bit input a
input [1:0] b; // 2-bit input b
output [2:0] sum; // 3-bit output sum
wire [2:0] sum;
assign sum = a + b; // Add inputs a and b
endmodule
```

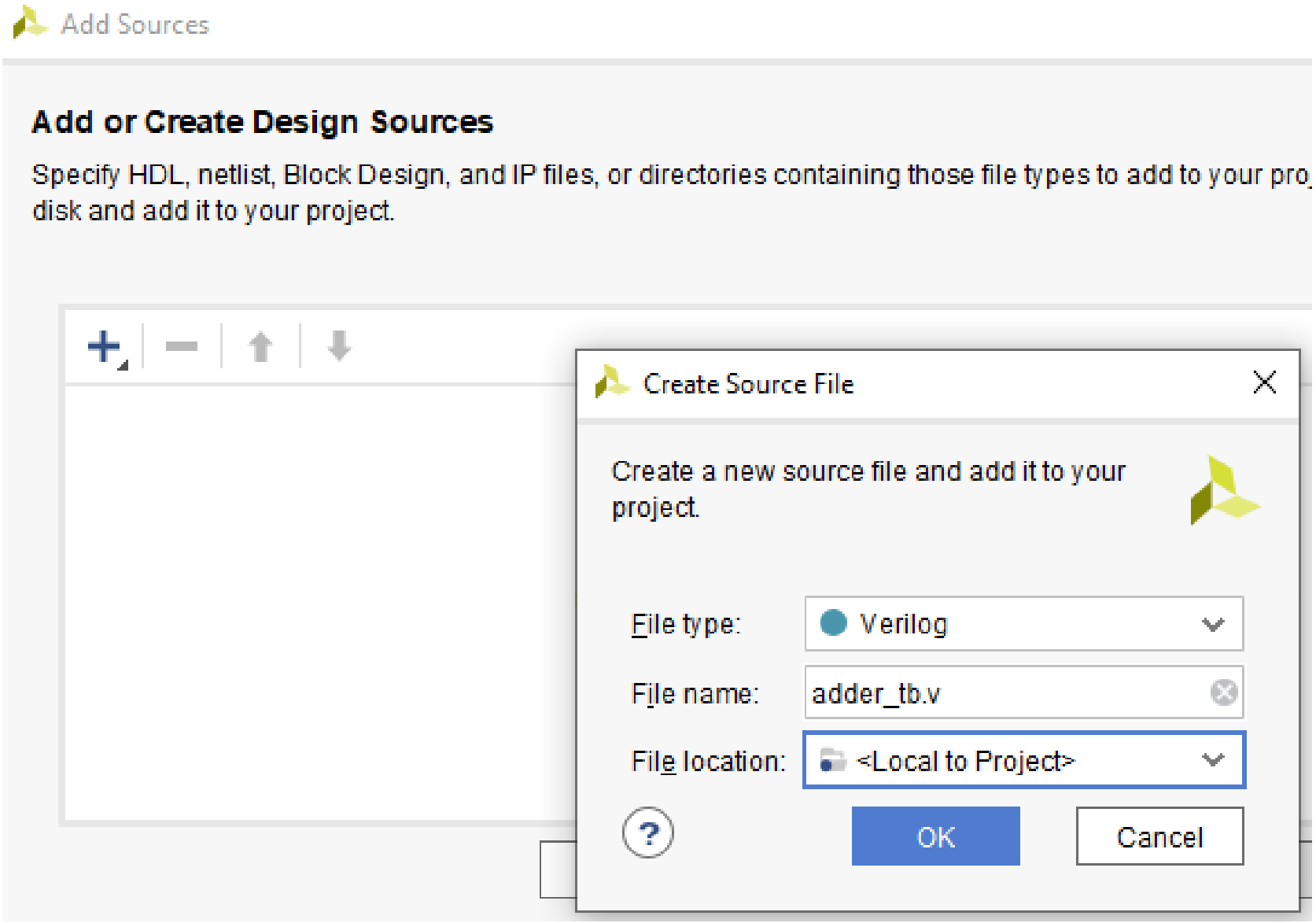

PROJECT MANAGER - adder
Sources
Design Sources (1)
Non-module Files (1)
sim_adder.v
Hierarchy
Libraries
Compile Order
Source File Properties
sim_adder.v
Enabled
General
Properties
Project Summary
sim_adder.v *
E:/UVM_project/adder/adder.srcs/sources_1/new/sim_adder
1 // A simple 2-bit adder
2 module sim_adder (a, b, sum);
3 input [1:0] a; // 2-bit input a
4 input [1:0] b; // 2-bit input b
5 output [2:0] sum; // 3-bit output sum
6 wire [2:0] sum;
7 assign sum = a + b; // Add inputs a and b
8 endmodule
9

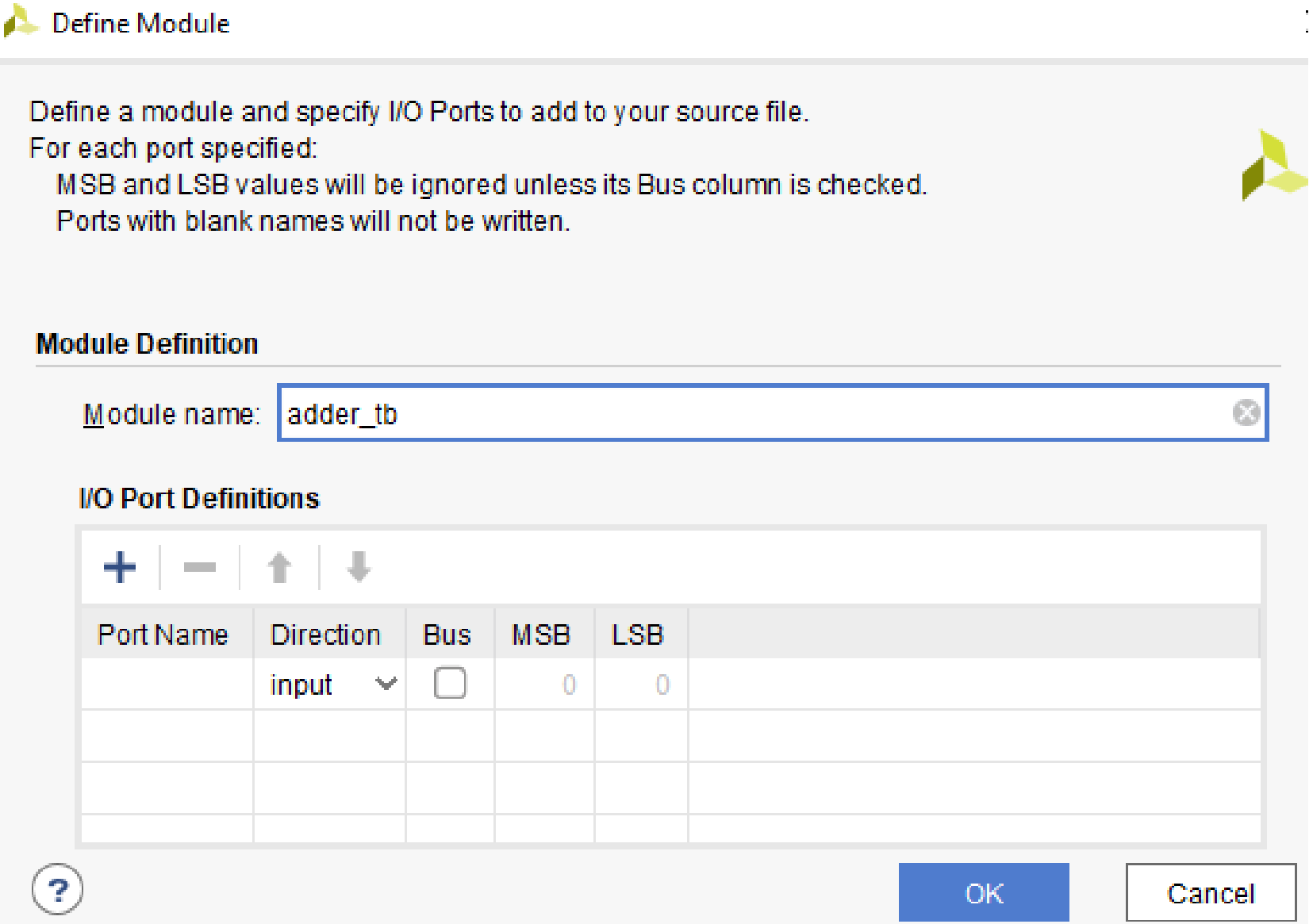
Create/Adding a Testbench File for Simulation

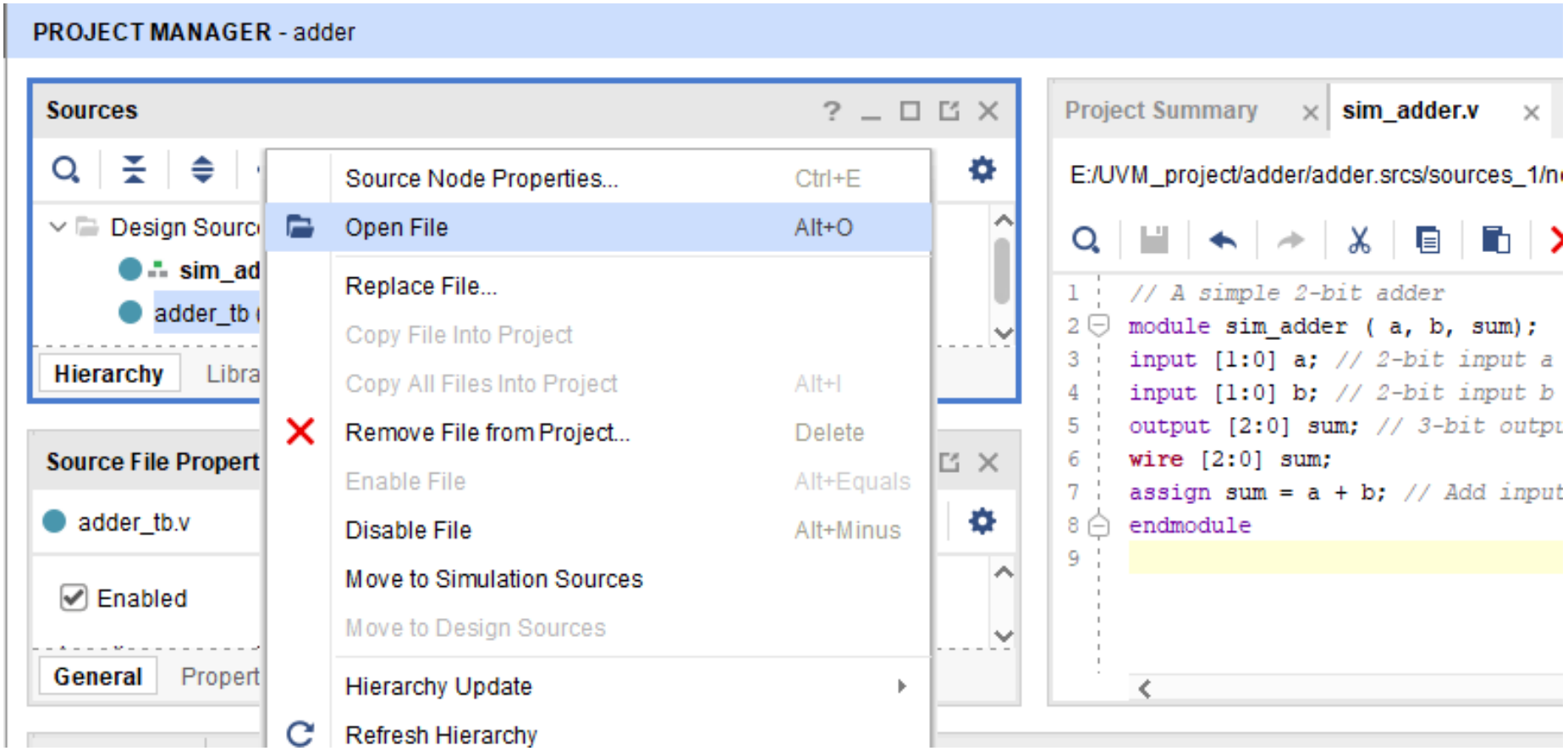
- In the **Project Manager**, click **Add Sources**.
- Select **Add or Create Simulation Sources** and click **Next**.
- Create a file named **adder_tb.v**, choose **Verilog**, and click **OK**.

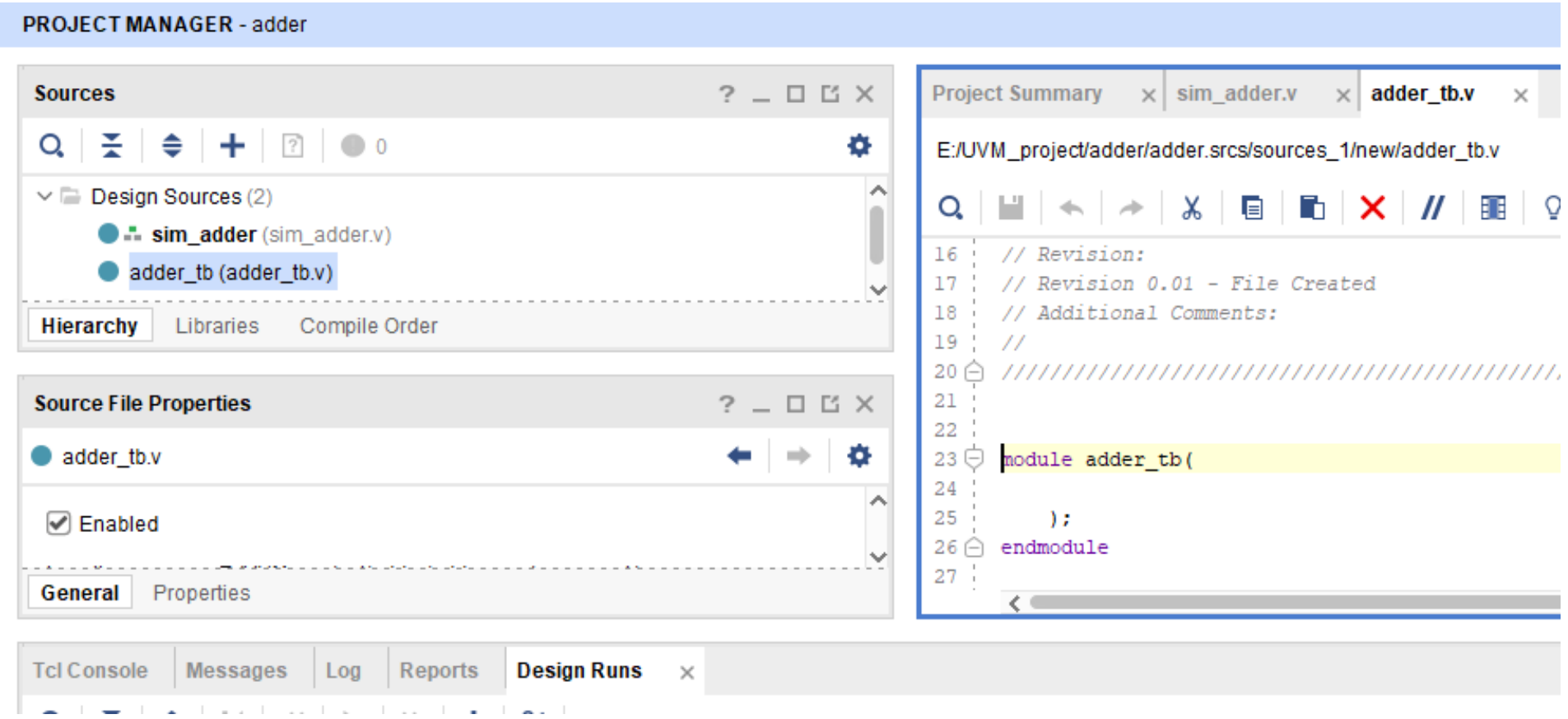
- Open **adder_tb.v** and add the testbench code.
  - (The testbench provides the inputs to test different cases of the 2-bit adder and prints the results.)
  - REF: https://medium.com/@techAsthetic/getting-started-with-rtl-design-using-xilinx-vivado-a-technical-guide-5a25ae03a594


PROJECT MANAGER - adder
Sources
Design Sources
Add Sources (Alt+A)
sim_adder
Constraints
Hierarchy
Libraries
Compile Order
Source File Properties
sim_adder.v
Enabled
General
Properties
Project Summary
sim_adder.v
E:/UVM_project/adder/adder.srcs/source
1 // A simple 2-bit adder
2 module sim_adder (a, b, su
3 input [1:0] a; // 2-bit inp
4 input [1:0] b; // 2-bit inp
5 output [2:0] sum; // 3-bit
6 wire [2:0] sum;
7 assign sum = a + b; // Add
8 endmodule
9


Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your pro
disk and add it to your project.
Create Source File
Create a new source file and add it to your project.
File type:
Verilog
File name:
adder_tb.v
File location:
<Local to Project>
OK
Cancel

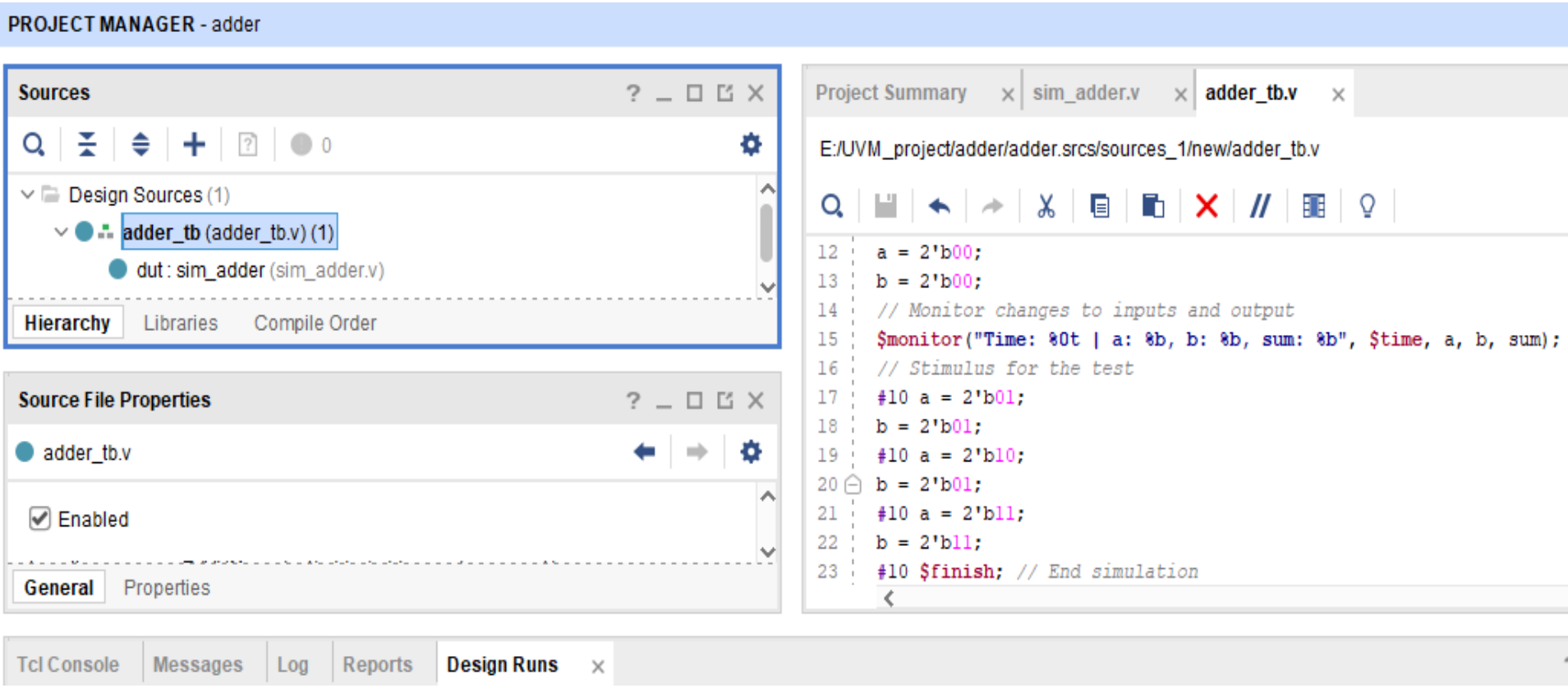

Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Module name:
adder_tb
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
input
0
0
OK
Cancel


PROJECT MANAGER - adder
Sources
Design Sourc
sim_ad
adder_tb
Hierarchy
Libra
Source File Propert
adder_tb.v
Enabled
General
Propert
Source Node Properties... Ctrl+E
Open File Alt+O
Replace File...
Copy File Into Project
Copy All Files Into Project Alt+I
Remove File from Project... Delete
Enable File Alt+Equals
Disable File Alt+Minus
Move to Simulation Sources
Move to Design Sources
Hierarchy Update
Refresh Hierarchy
Project Summary
sim_adder.v
E:/UVM_project/adder/adder.srcs/sources_1/n
1 // A simple 2-bit adder
2 module sim_adder (a, b, sum);
3 input [1:0] a; // 2-bit input a
4 input [1:0] b; // 2-bit input b
5 output [2:0] sum; // 3-bit outpu
6 wire [2:0] sum;
7 assign sum = a + b; // Add input
8 endmodule
9


PROJECT MANAGER - adder
Sources
Design Sources (2)
sim_adder (sim_adder.v)
adder_tb (adder_tb.v)
Hierarchy
Libraries
Compile Order
Source File Properties
adder_tb.v
Enabled
General
Properties
Project Summary
sim_adder.v
adder_tb.v
E:/UVM_project/adder/adder.srcs/sources_1/new/adder_tb.v
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21
22
23 module adder_tb(
24
25);
26 endmodule
27
Tcl Console
Messages
Log
Reports
Design Runs

Creating/Adding a Testbench for Simulation

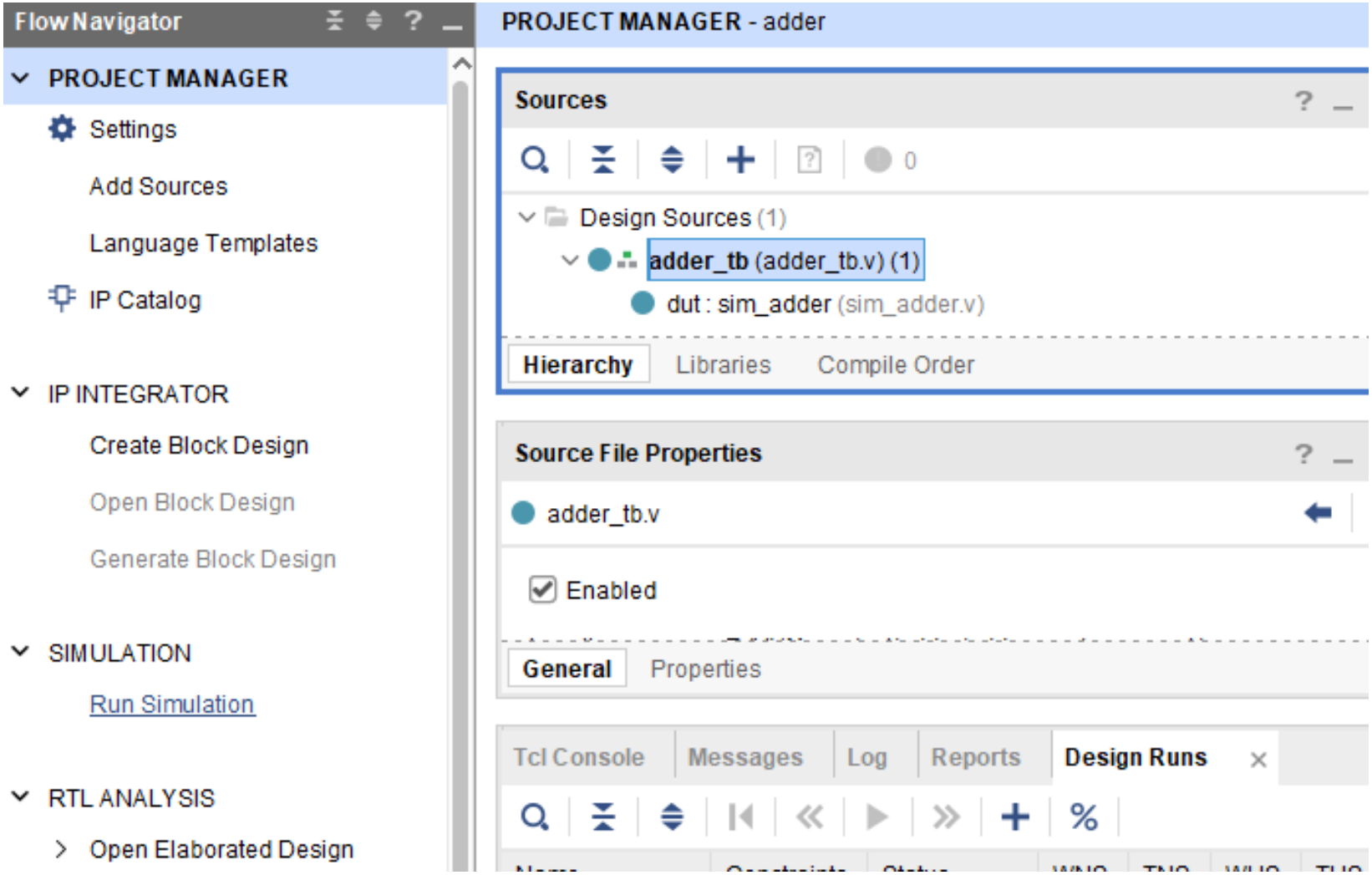
```
`timescale 1ns/1ps
module adder_tb;
reg [1:0] a;
reg [1:0] b;
wire [2:0] sum;
// Instantiate the simple_adder module
sim_adder dut ( .a(a),
                .b(b),
                .sum(sum));
initial begin
// Initialize inputs
a = 2'b00;
b = 2'b00;
// Monitor changes to inputs and output
$monitor("Time: %0t | a: %b, b: %b, sum:
    %b", $time, a, b, sum);
// Stimulus for the test
#10 a = 2'b01;
b = 2'b01;
#10 a = 2'b10;
b = 2'b01;
#10 a = 2'b11;
b = 2'b11;
#10 $finish; // End simulation
end
endmodule
```

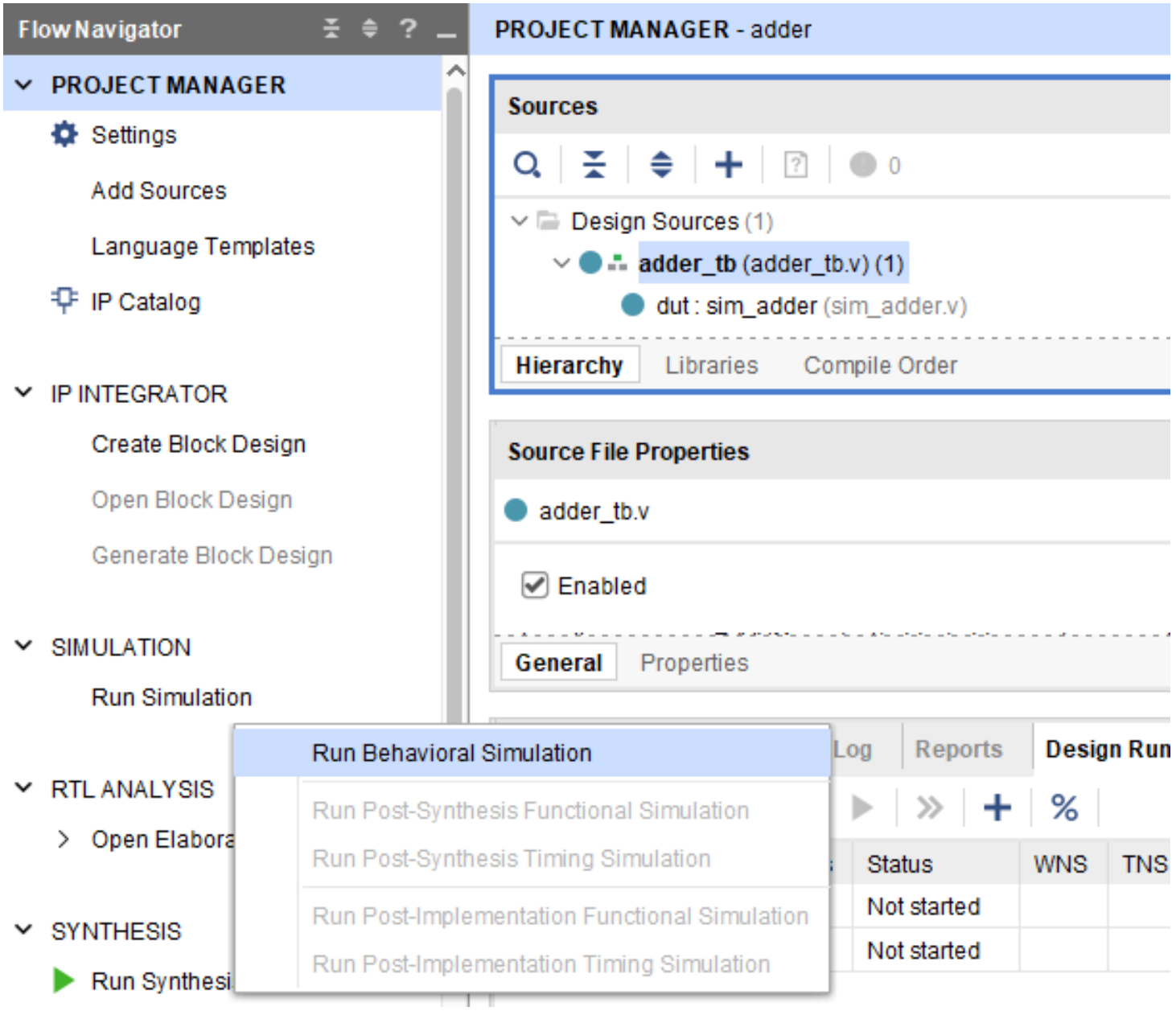

PROJECT MANAGER - adder
Sources
Design Sources (1)
adder_tb (adder_tb.v) (1)
dut : sim_adder (sim_adder.v)
Hierarchy
Libraries
Compile Order
Source File Properties
adder_tb.v
Enabled
General
Properties
Project Summary
sim_adder.v
adder_tb.v
E:/UVM_project/adder/adder.srcs/sources_1/new/adder_tb.v
12 a = 2'b00;
13 b = 2'b00;
14 // Monitor changes to inputs and output
15 $monitor("Time: %0t | a: %b, b: %b, sum: %b", $time, a, b, sum);
16 // Stimulus for the test
17 #10 a = 2'b01;
18 b = 2'b01;
19 #10 a = 2'b10;
20 b = 2'b01;
21 #10 a = 2'b11;
22 b = 2'b11;
23 #10 $finish; // End simulation
Tcl Console
Messages
Log
Reports
Design Runs

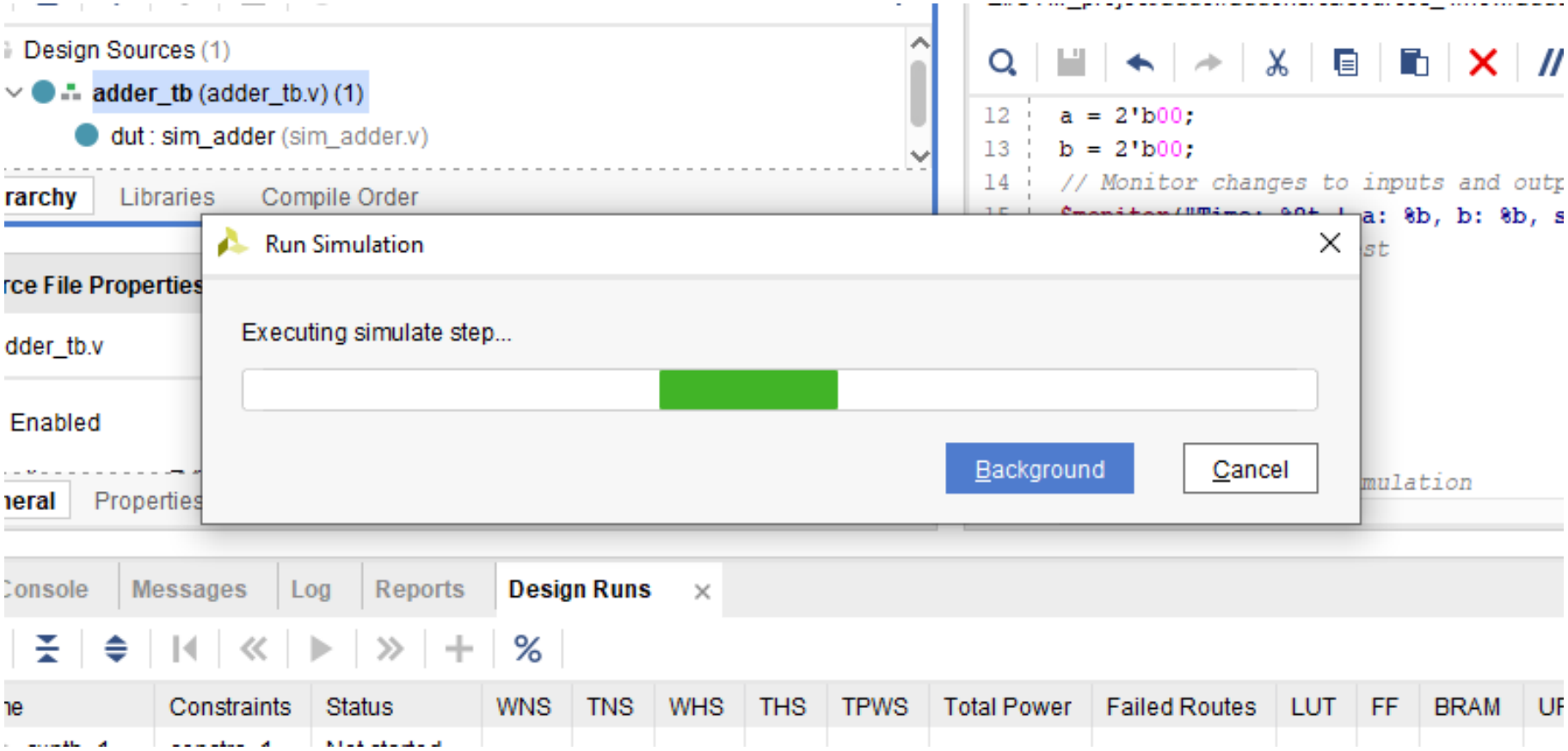
Simulating the RTL Design

Simulation

- In the **Flow Navigator**, under **Simulation**, click **Run Simulation** and select **Run Behavioral Simulation**.


Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
PROJECT MANAGER - adder
Sources
0
Design Sources (1)
adder_tb (adder_tb.v) (1)
dut : sim_adder (sim_adder.v)
Hierarchy
Libraries
Compile Order
Source File Properties
adder_tb.v
Enabled
General
Properties
Tcl Console
Messages
Log
Reports
Design Runs


Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elabora
SYNTHESIS
Run Synthesi
PROJECT MANAGER - adder
Sources
0
Design Sources (1)
adder_tb (adder_tb.v) (1)
dut : sim_adder (sim_adder.v)
Hierarchy
Libraries
Compile Order
Source File Properties
adder_tb.v
Enabled
General
Properties
Run Behavioral Simulation
Run Post-Synthesis Functional Simulation
Run Post-Synthesis Timing Simulation
Run Post-Implementation Functional Simulation
Run Post-Implementation Timing Simulation
Log
Reports
Design Run
Status
WNS
TNS
Not started
Not started


Design Sources (1)
adder_tb (adder_tb.v) (1)
dut : sim_adder (sim_adder.v)
rarchy
Libraries
Compile Order
rce File Properties
dder_tb.v
Enabled
neral
Properties
12 a = 2'b00;
13 b = 2'b00;
14 // Monitor changes to inputs and outp
a: %b, b: %b, s
st
mulation
Run Simulation
Executing simulate step...
Background
Cancel
Console
Messages
Log
Reports
Design Runs
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAM

Thank You