ASIC/FPGA Design and Verification

Part 1: FPGA Technology

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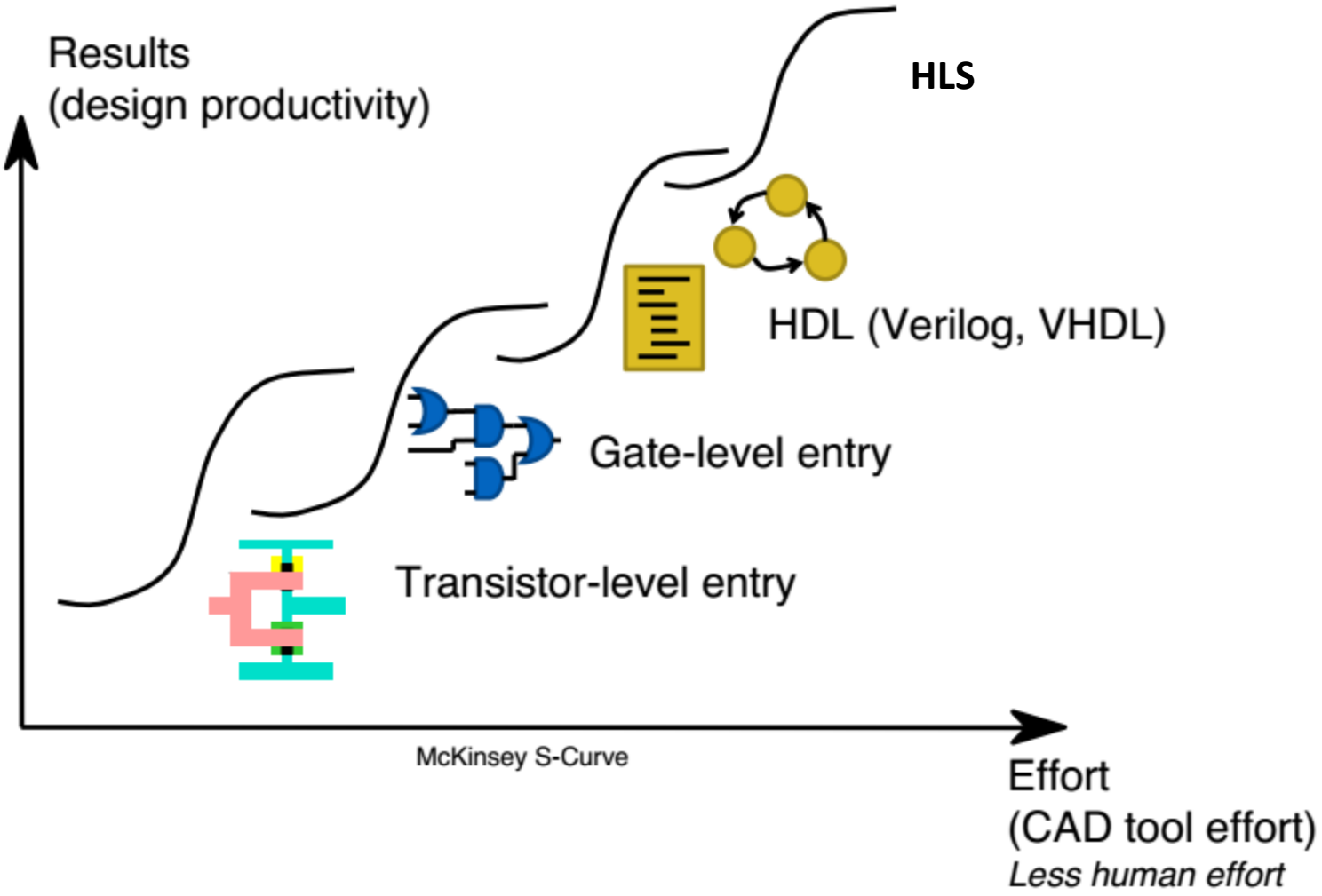
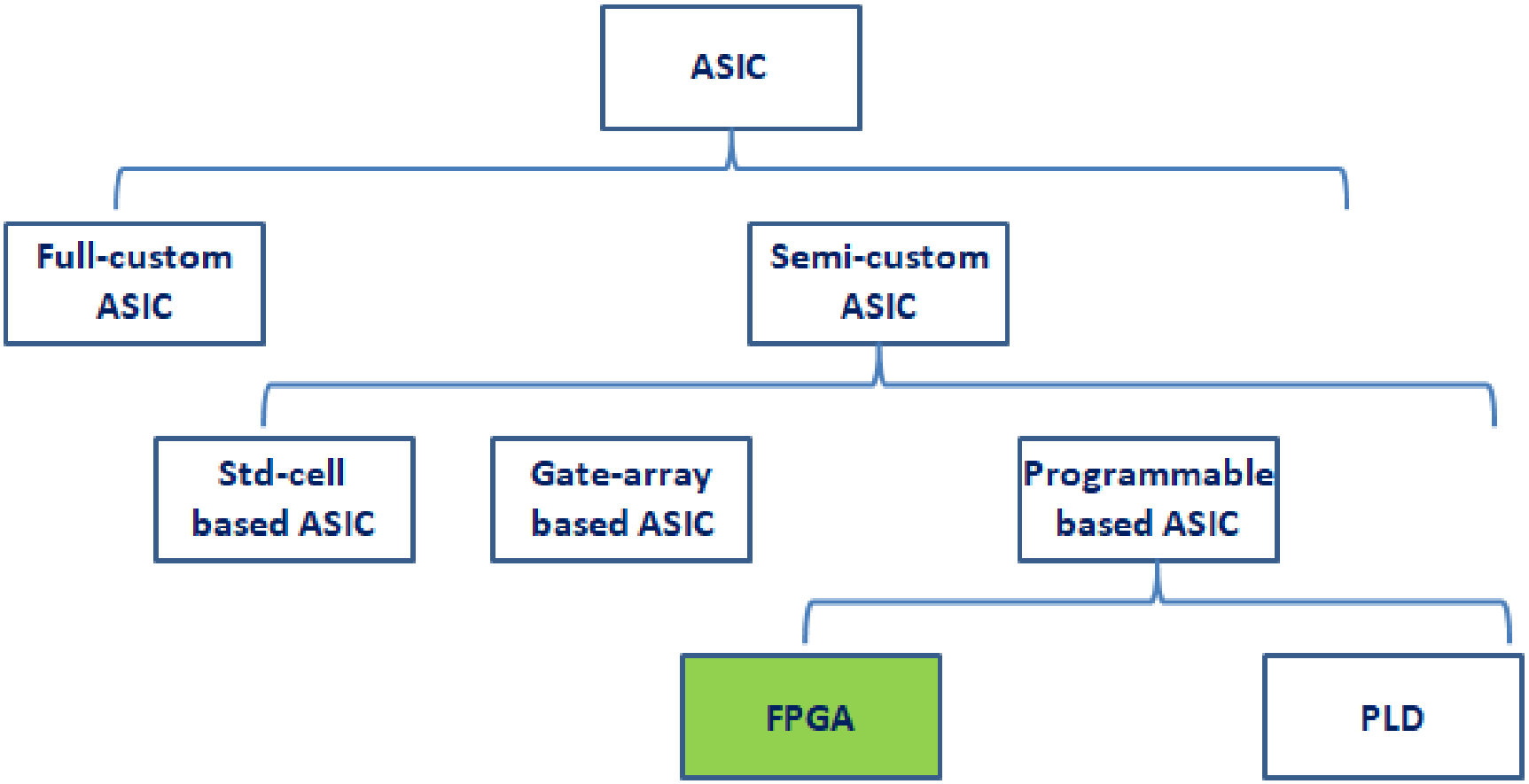
Design Abstraction Levels

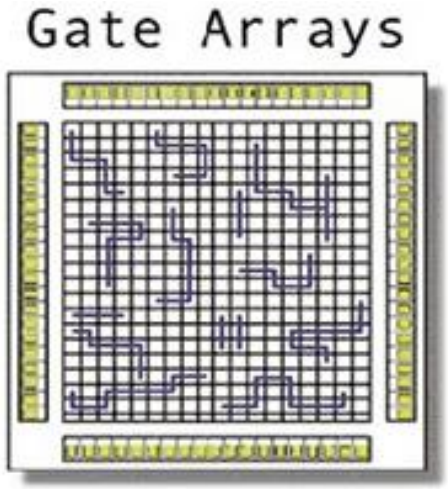


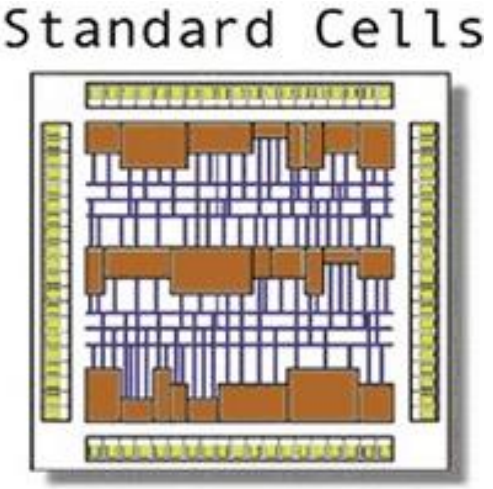
ASIC Types

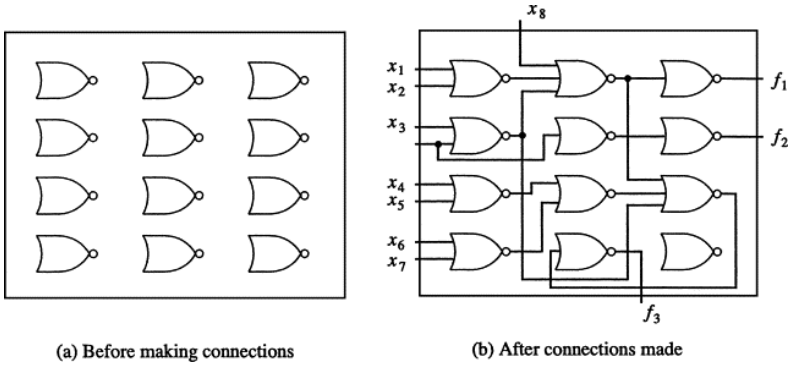

ASIC
Full-custom ASIC
Semi-custom ASIC
Std-cell based ASIC
Gate-array based ASIC
Programmable based ASIC
FPGA
PLD

Basic Building Block

A gate array is logic gates that are pre-laid in matrix form on a chip.





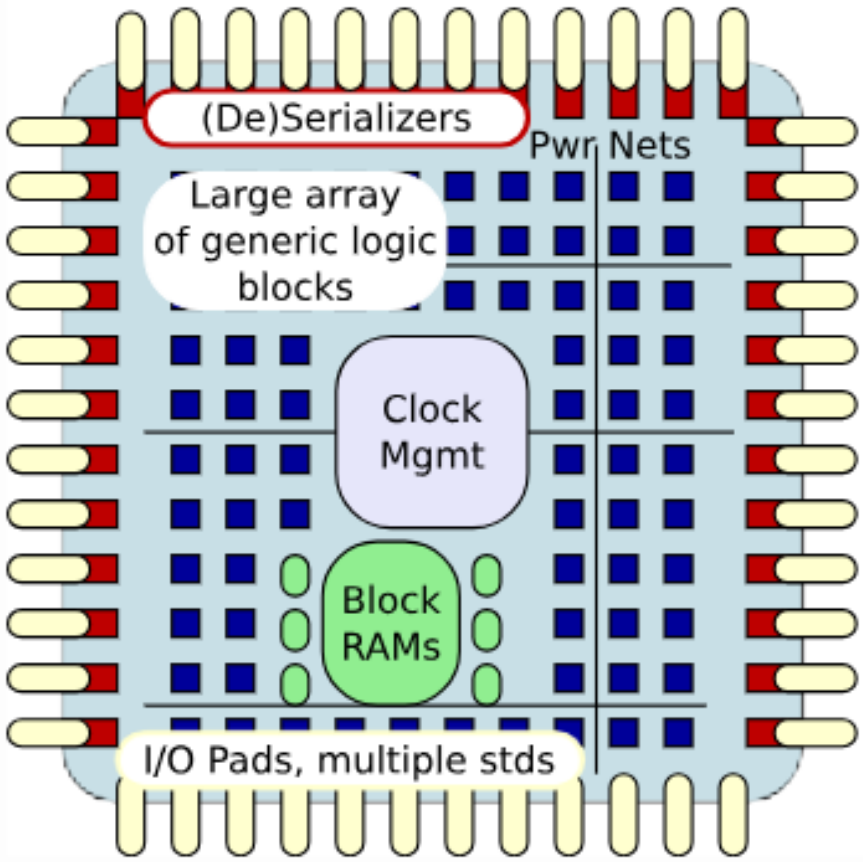


(a) Before making connections

(b) After connections made

A standard cell is **group of transistor and interconnect structures**, which provides a boolean logic function (e.g., AND, OR, XOR, XNOR, inverters) … A standard cell is a **pre-designed and pre-verified building block**. Standard cell libraries are **a set of cells that have common characteristics and physical layout**.

ASIC/FPGA Development



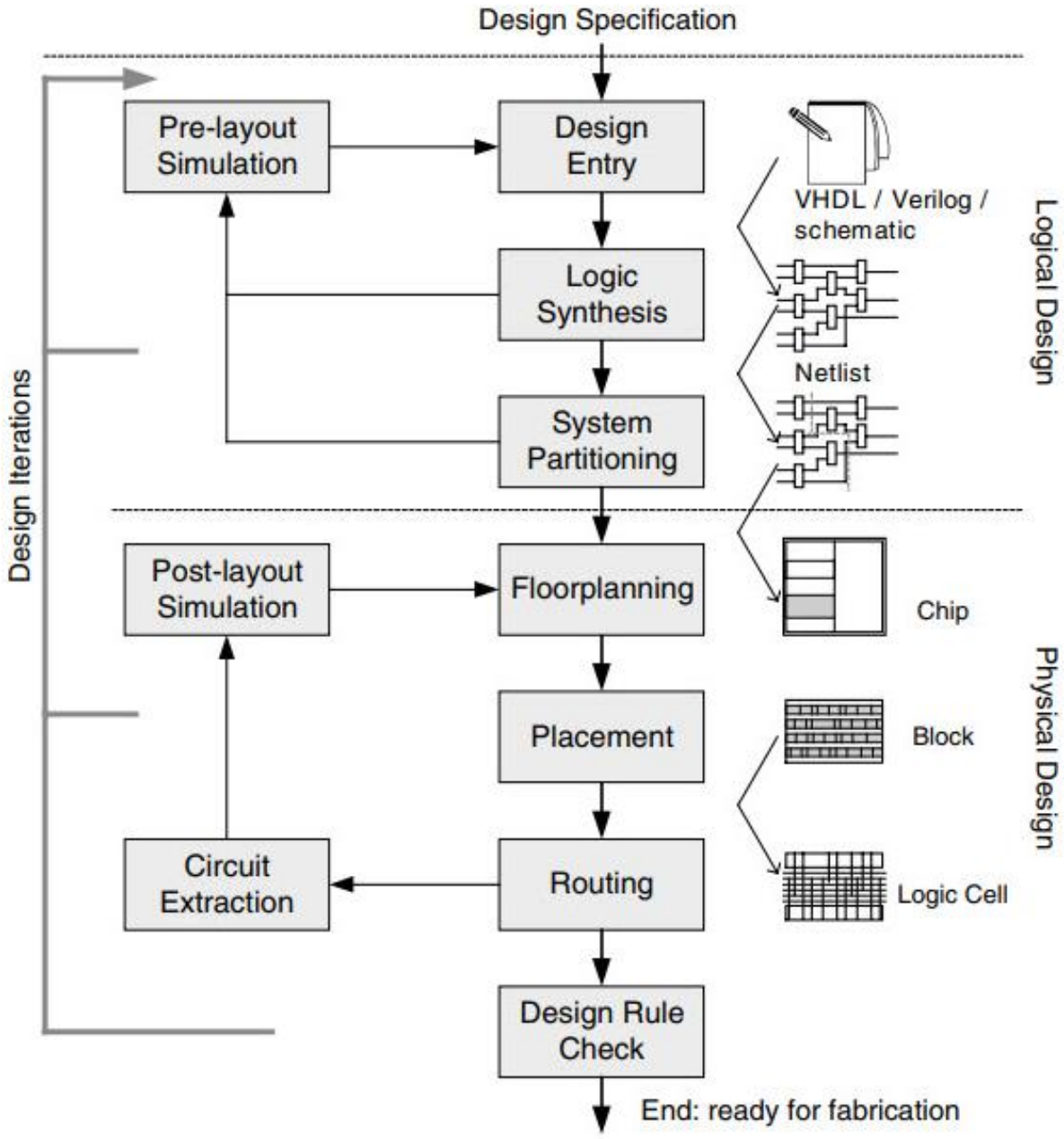
ASIC Design starts with a blank tableau

You need to add the components you need/want

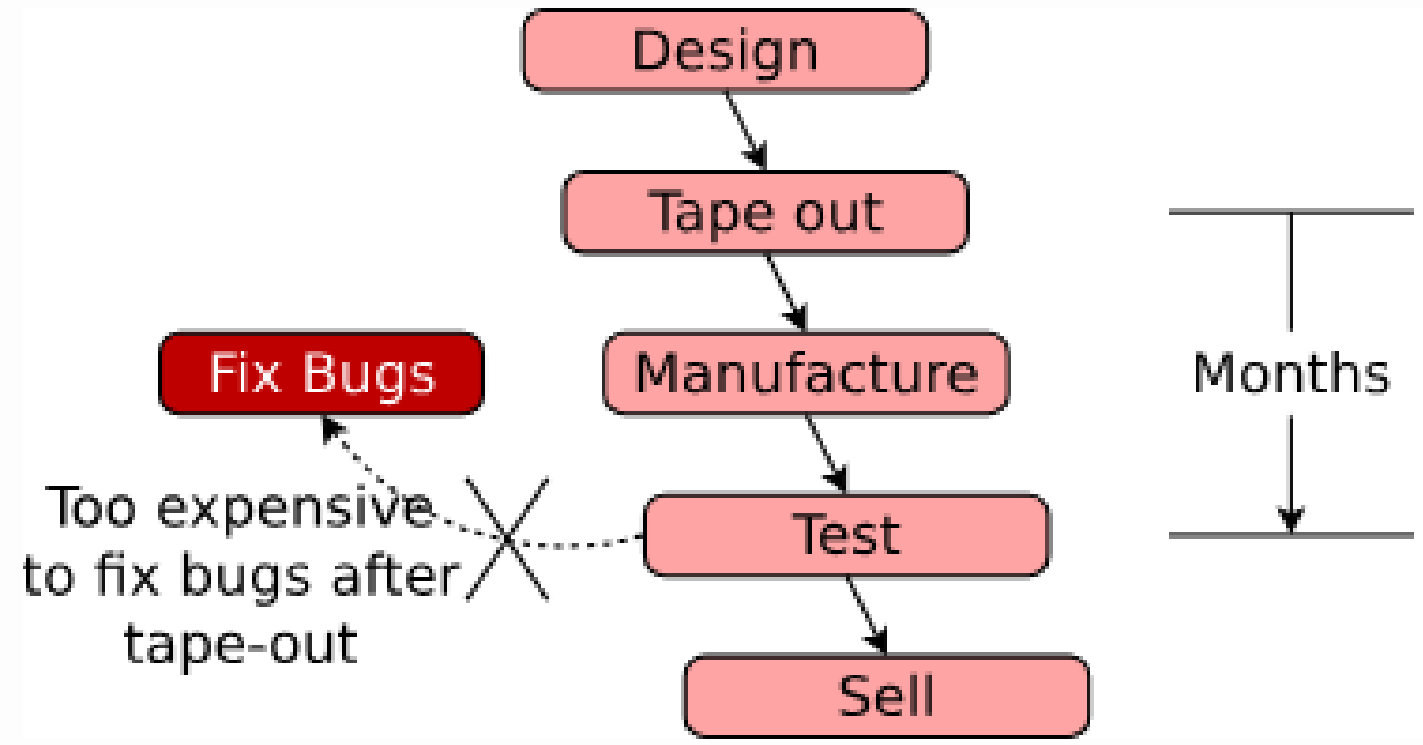
FPGA

ASIC

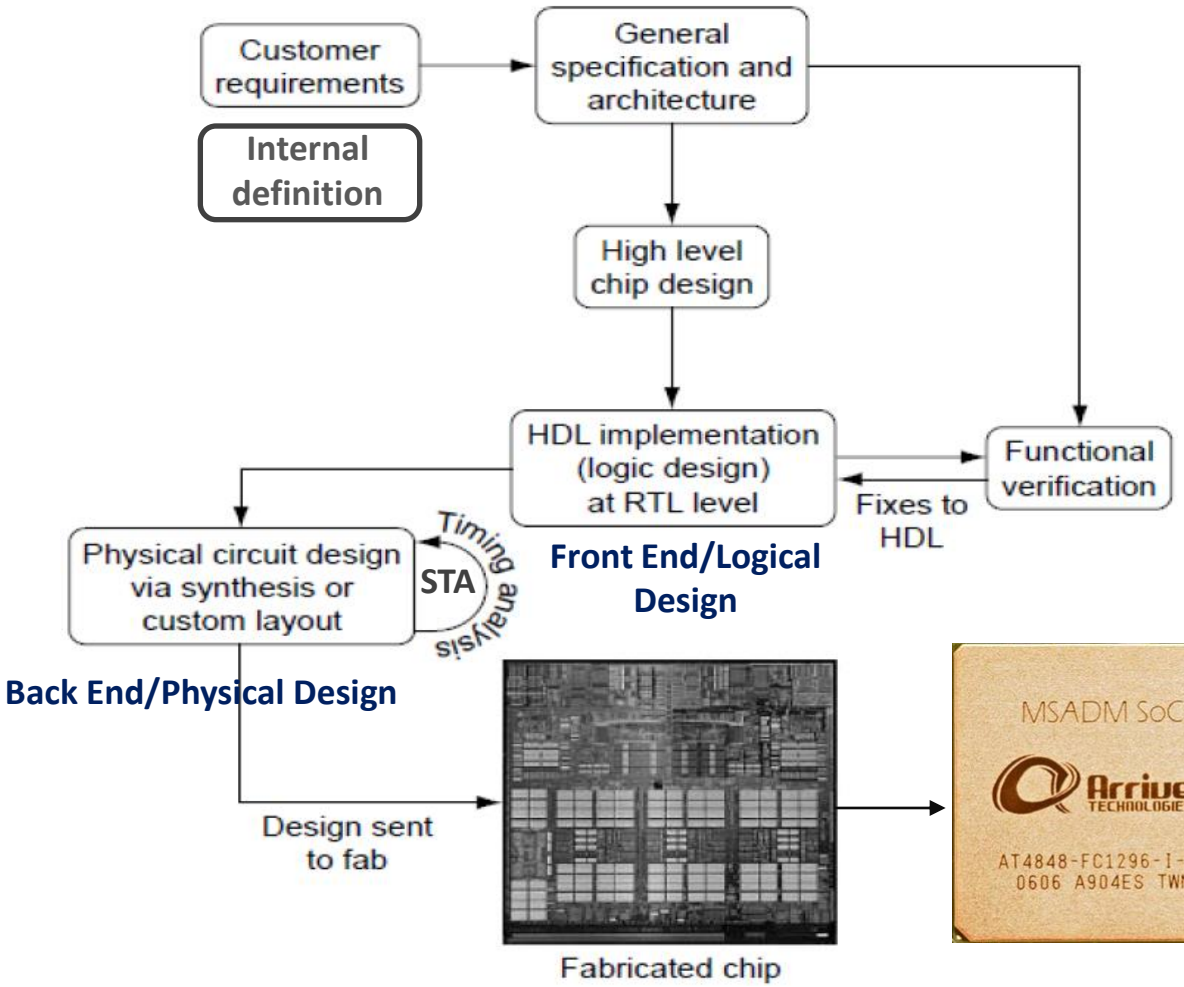
ASIC Design Flow



P-D-C-A: ASIC Design

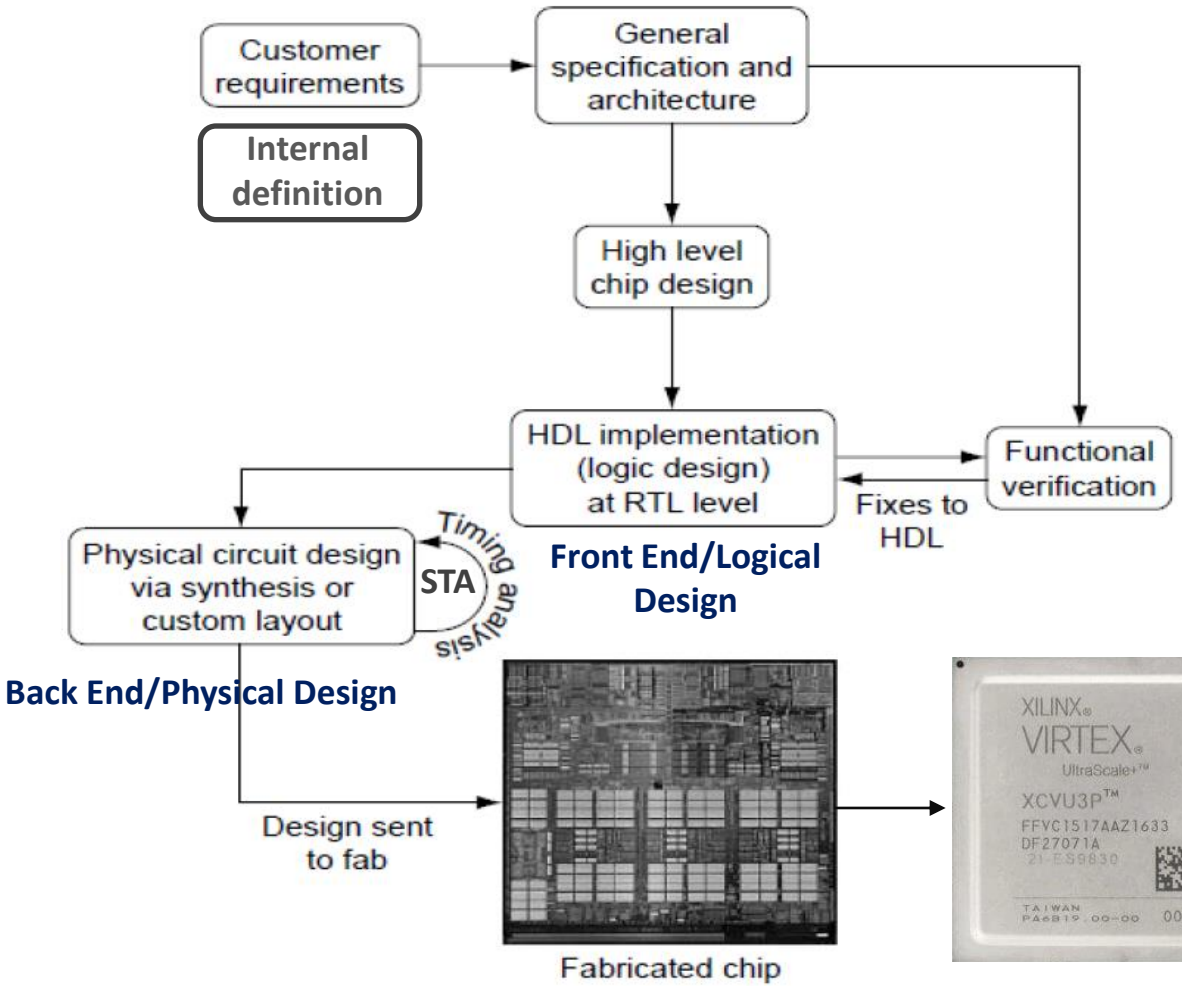


ASIC Design Flow for a Specific Application

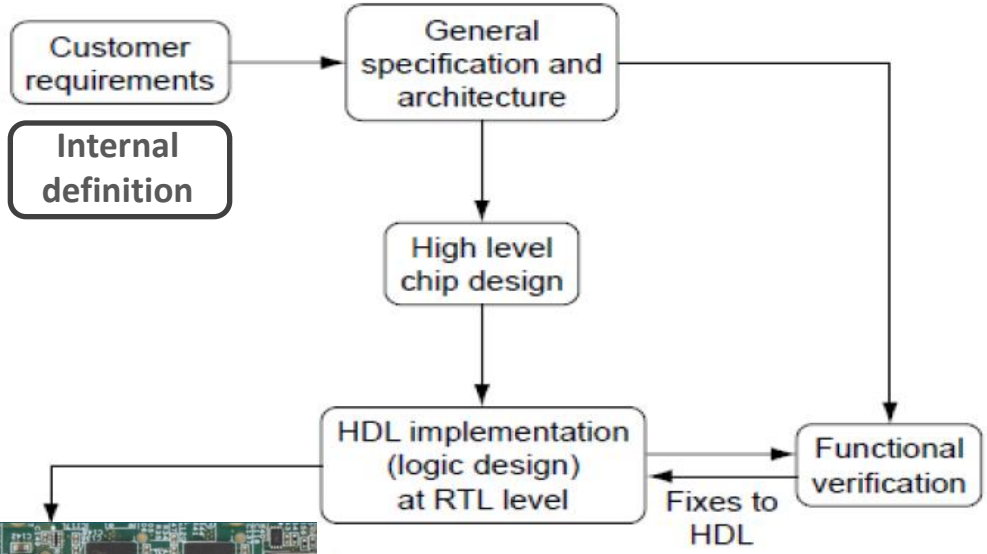


ASIC – **A**pplication **S**pecific **IC**

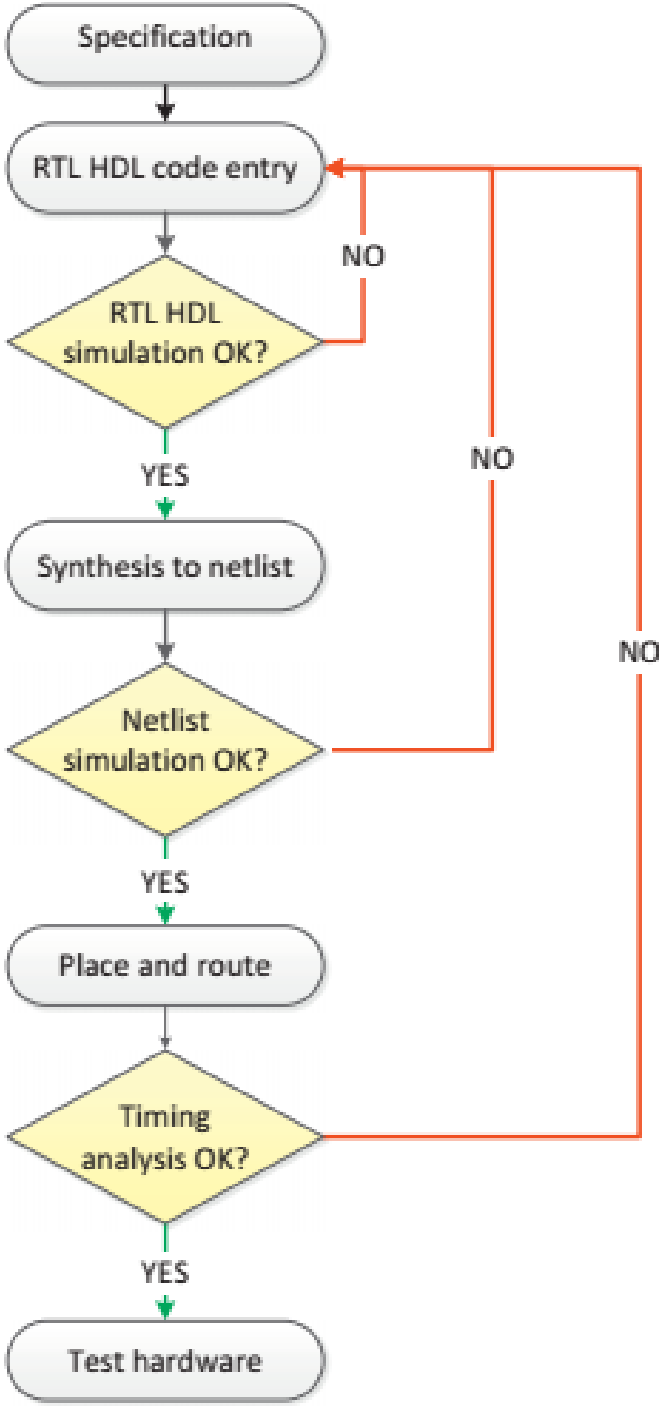
ASIC Design Flow for an FPGA



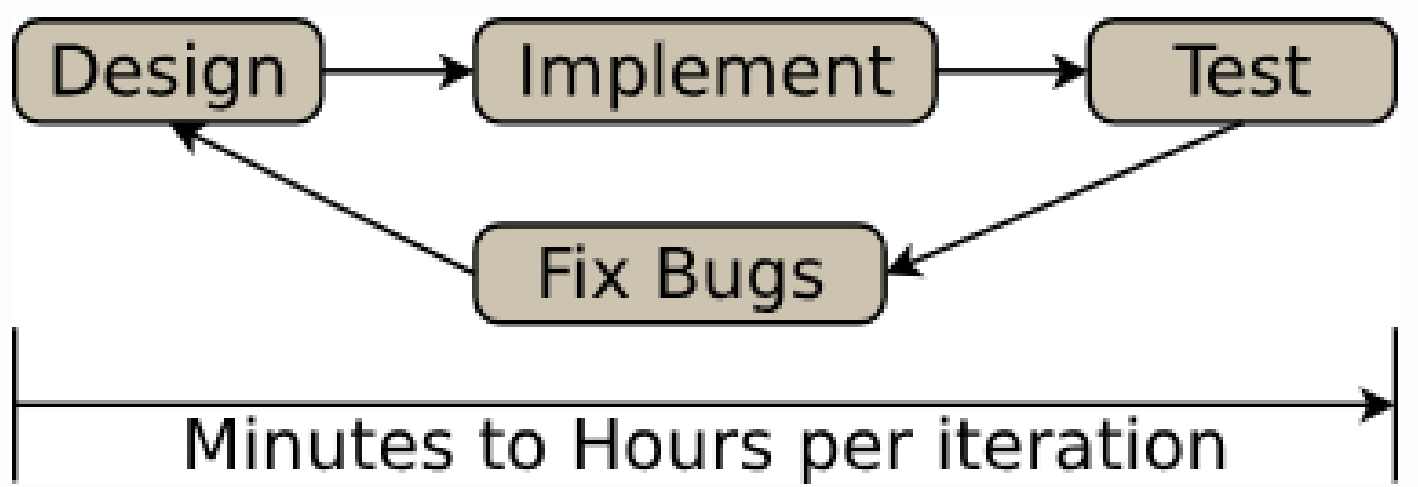
FPGA based Chip Design Flow



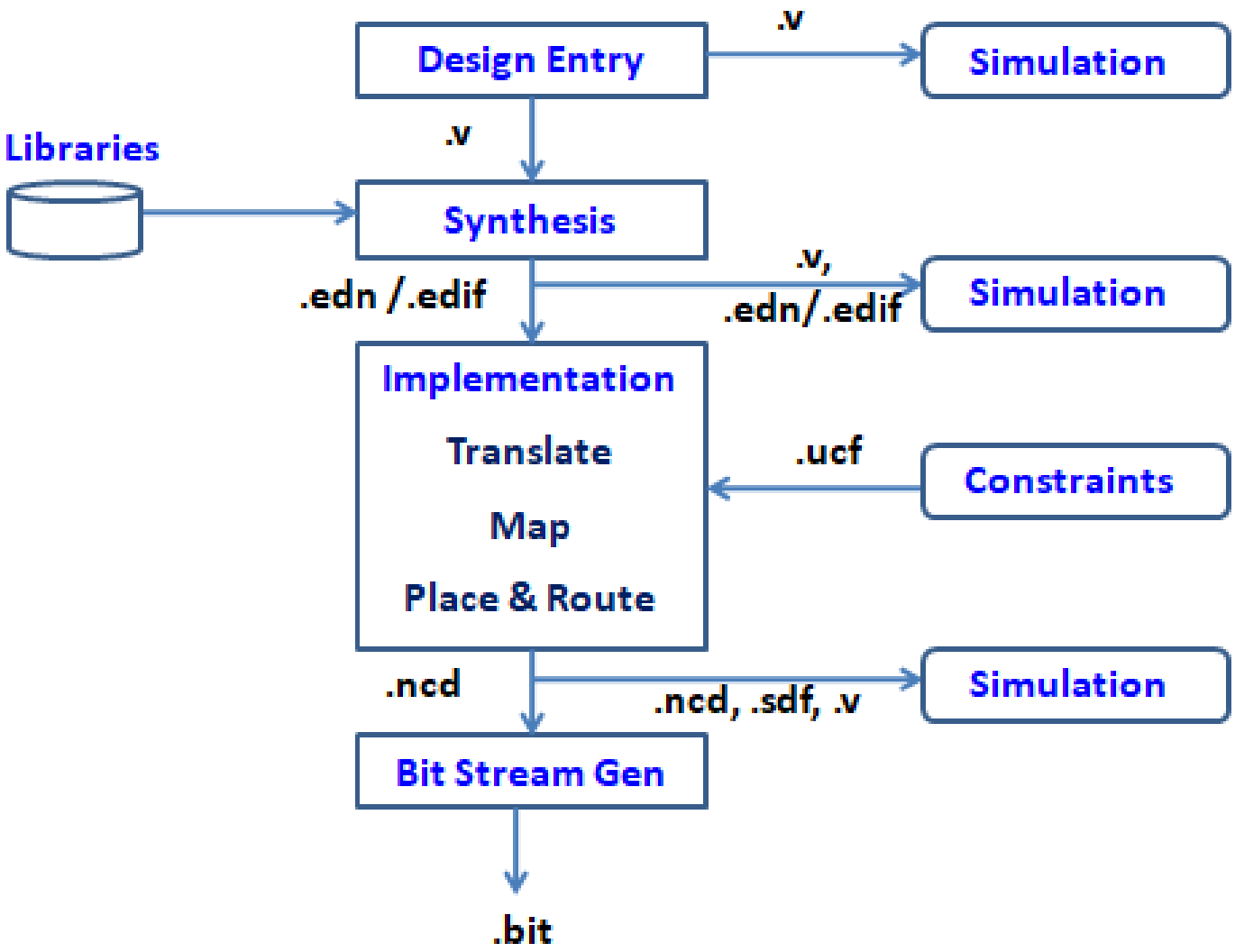
FPGA based Design Flow



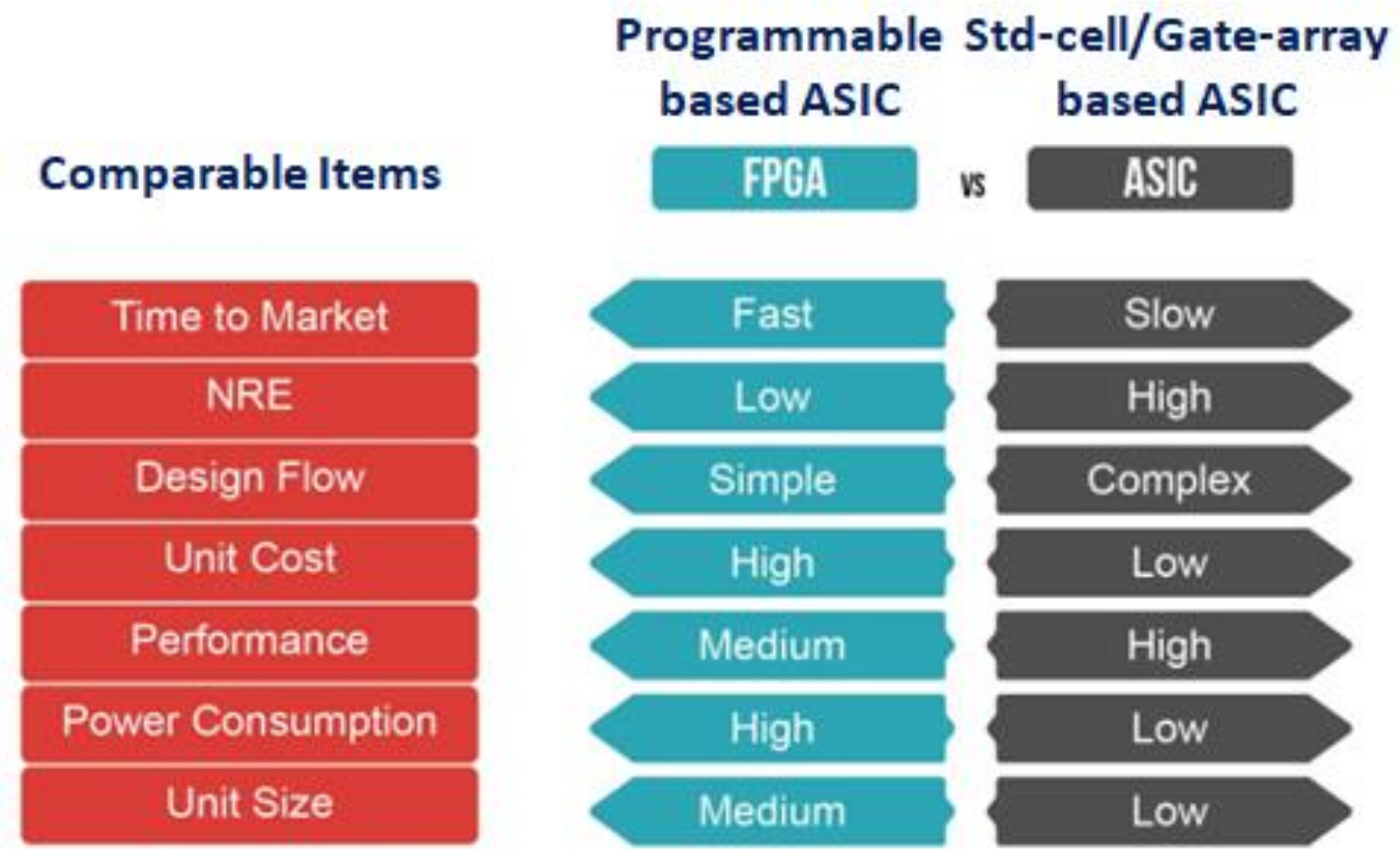
P-D-C-A: FPGA based Design



An Example Simulation Flow



FPGA vs ASIC


Programmable based ASIC
Std-cell/Gate-array based ASIC
Comparable Items
FPGA
vs
ASIC
Time to Market
Fast
Slow
NRE
Low
High
Design Flow
Simple
Complex
Unit Cost
High
Low
Performance
Medium
High
Power Consumption
High
Low
Unit Size
Medium
Low

Thank You