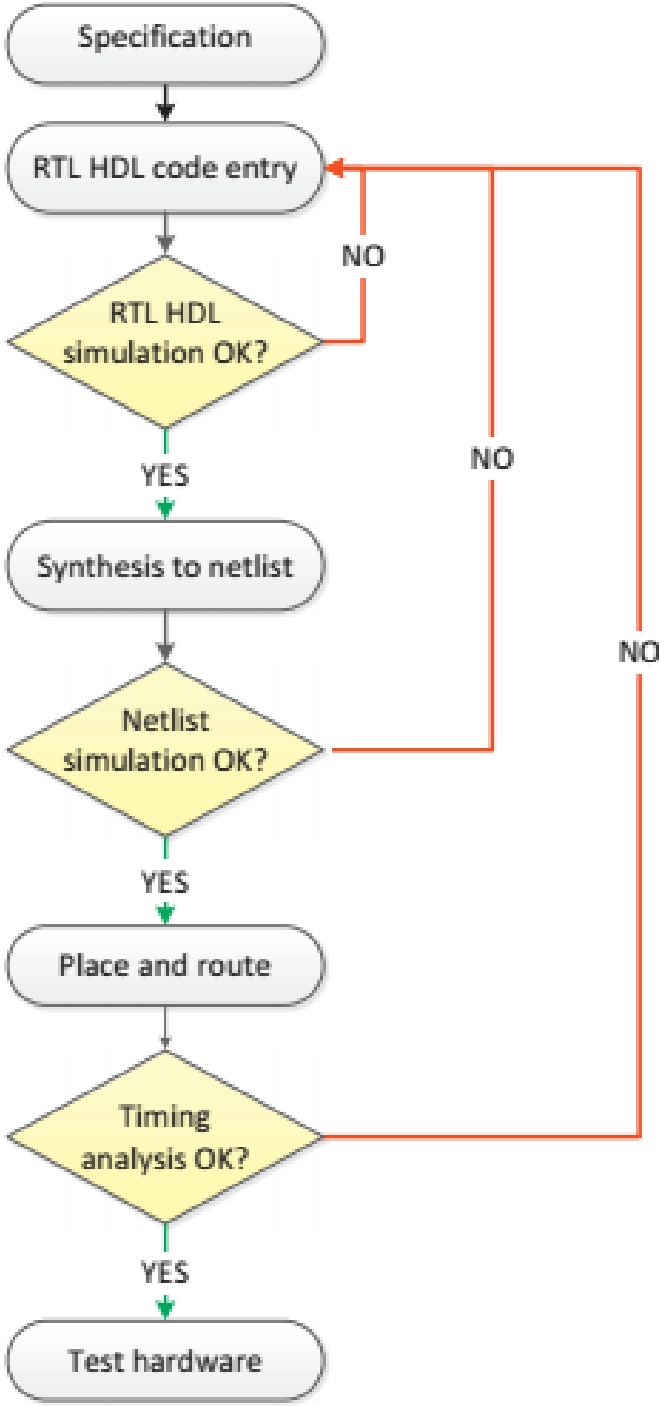
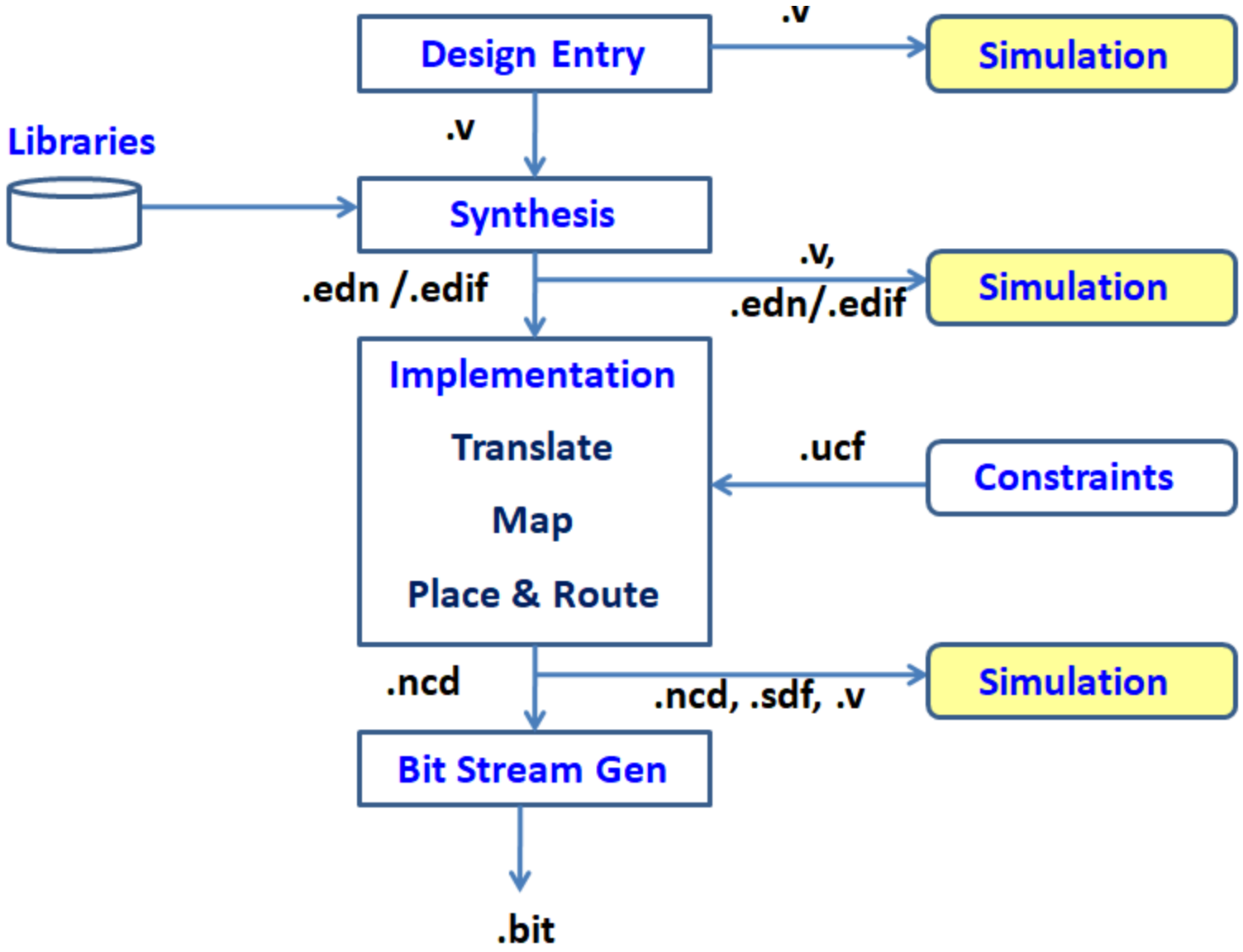
ASIC/FPGA Design and Verification

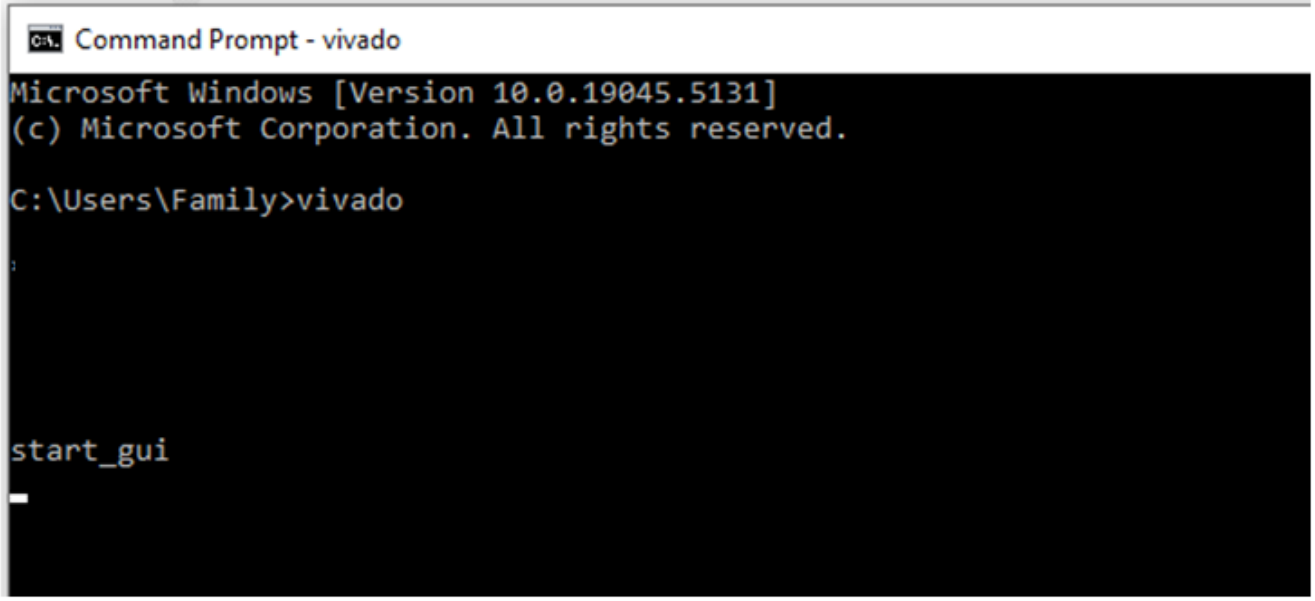
Part 3: Using Command Line

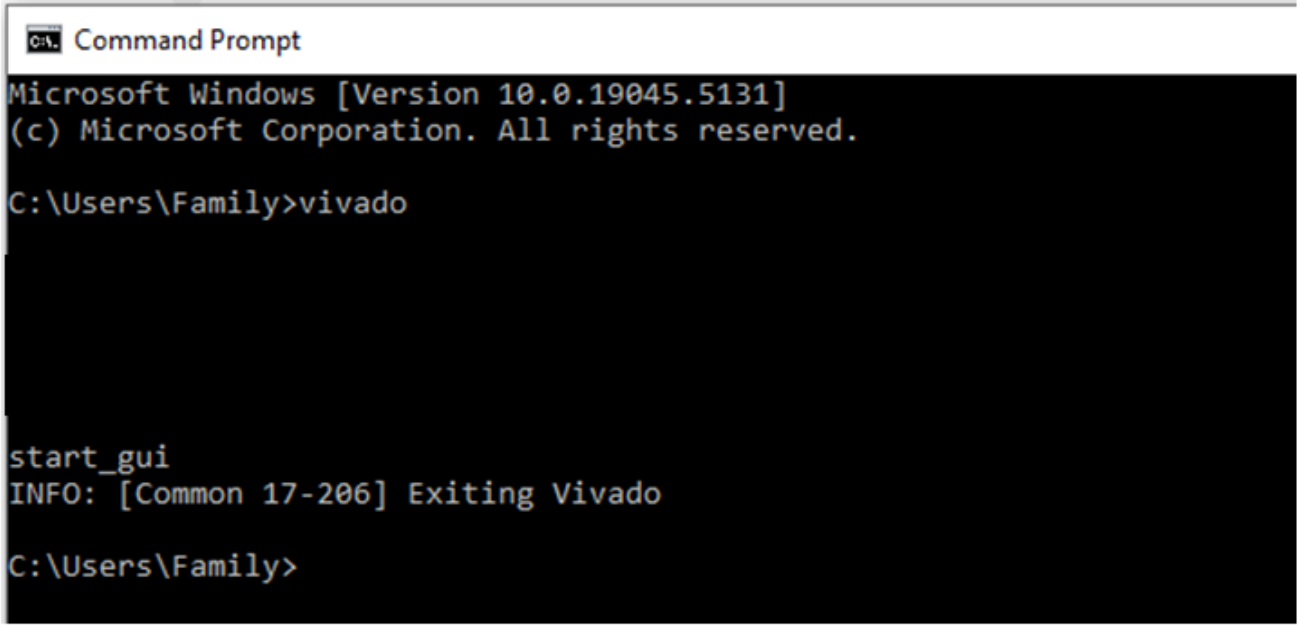
Tuan Nguyen-viet


Specification
RTL HDL code entry
RTL HDL simulation OK?
NO
YES
Synthesis to netlist
Netlist simulation OK?
NO
YES
Place and route
Timing analysis OK?
NO
YES
Test hardware


Design Entry
.v
Simulation
Libraries
.v
Synthesis
.edn /.edif
.v,
.edn/.edif
Simulation
Implementation
Translate
Map
Place & Route
.ucf
Constraints
.ncd
.ncd, .sdf, .v
Simulation
Bit Stream Gen
.bit

GUI (see Slide _P2)





RTL Design Verification

CMD Line

★ **Tip:** To add the Vivado tools path to your current shell/command prompt, run `settings64.bat` or `settings64.sh` from the <install_path>/Vivado/<version> directory.

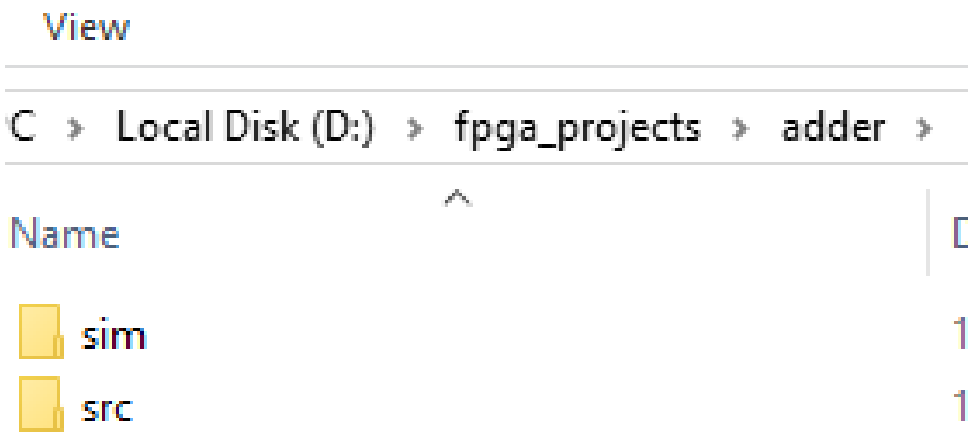
Before we can run a script from the command line,
we need to source the Vivado environment.

On **Windows** run the batch script from a command prompt:

C:/Xilinx/Vivado/<version>/settings64.bat

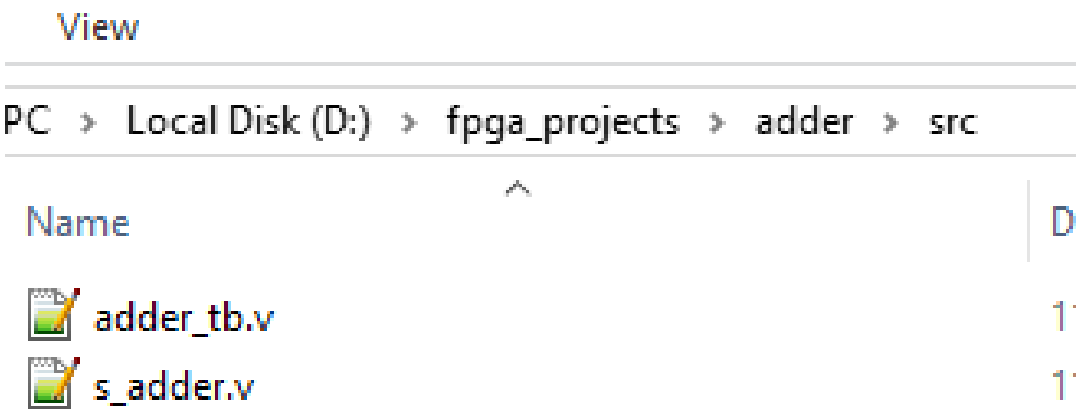
Replace " <version> " with a Vivado version, such as 2022.2.

REF: https://docs.amd.com/r/en-US/ug892-vivado-design-flows-overview/Launching-the-Vivado-IDE-on-Windows


View
C
Local Disk (D:)
fpga_projects
adder
Name
sim
src

```
/*
// A simple 2-bit adder
module s_adder ( a, b, sum);
input [1:0] a; // 2-bit input a
input [1:0] b; // 2-bit input b
output [2:0] sum; // 3-bit output sum
wire [2:0] sum;
assign sum = a + b; // Add inputs a and b
endmodule
*/
`timescale 1ns / 1ps
// A simple 32-bit adder
module s_adder (a, b, sum);
input [31:0] a; // 32-bit input a
input [31:0] b; // 32-bit input b
output [31:0] sum; // 32-bit output sum
reg [31:0] sum;

always @ (a or b) begin
        sum = a + b; // Add inputs a and b
end

endmodule
```

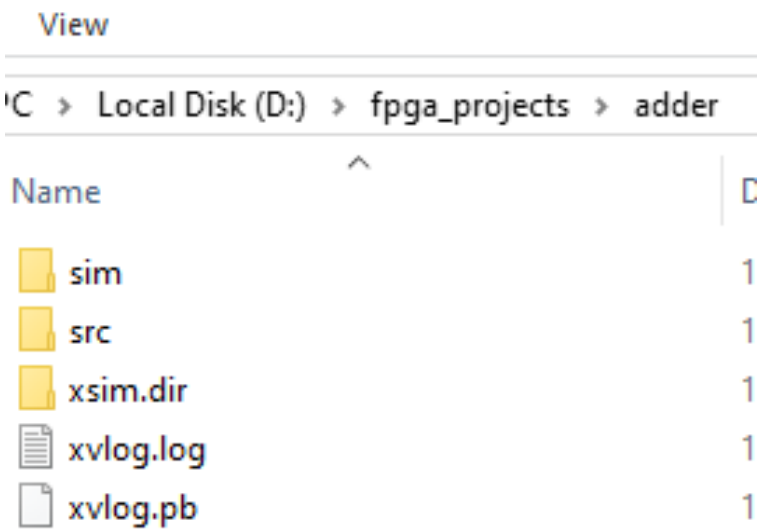
```
`timescale 1ns / 1ps
module adder_tb;
reg [31:0] a;
reg [31:0] b;
wire [31:0] sum;
// Instantiate the simple_adder module
s_adder dut ( .a(a),
              .b(b),
              .sum(sum));
initial begin
// Initialize inputs
a = 32'b00;
b = 32'b00;
// Monitor changes to inputs and output
$monitor("Time: %0t | a: %b, b: %b, sum: %b", $time, a, b, sum);
// Stimulus for the test
#10 a = 32'b01;
b = 32'b01;
#10 a = 32'b10;
b = 32'b01;
#10 a = 32'b11;
b = 32'b11;
#10 $finish; // End simulation
end
endmodule
```


View
PC › Local Disk (D:) › fpga_projects › adder › src
Name
D
adder_tb.v
1
s_adder.v
1

Compilation

```
C:\Users\Family>d:

D:\>cd D:\fpga_projects\adder\
```

```
D:\fpga_projects\adder>xvlog ./src/s_adder.v ./src/adder_tb.v
INFO: [VRFC 10-2263] Analyzing Verilog file "D:/fpga_projects/adder/src/s_adder.v" into library work
INFO: [VRFC 10-311] analyzing module s_adder
INFO: [VRFC 10-2263] Analyzing Verilog file "D:/fpga_projects/adder/src/adder_tb.v" into library work
INFO: [VRFC 10-311] analyzing module adder_tb

D:\fpga_projects\adder>cd sim
```



```
D:\fpga_projects\adder\sim>xvlog ../src/s_adder.v ../src/adder_tb.v
INFO: [VRFC 10-2263] Analyzing Verilog file "D:/fpga_projects/adder/src/s_adder.v" into library work
INFO: [VRFC 10-311] analyzing module s_adder
INFO: [VRFC 10-2263] Analyzing Verilog file "D:/fpga_projects/adder/src/adder_tb.v" into library work
INFO: [VRFC 10-311] analyzing module adder_tb

D:\fpga_projects\adder\sim>
```

Compiled Design Elaboration / Built Simulation

```
D:\fpga_projects\adder\sim>xvlog ../src/s_adder.v ../src/adder_tb.v
INFO: [VRFC 10-2263] Analyzing Verilog file "D:/fpga_projects/adder/src/s_adder.v" into library work
INFO: [VRFC 10-311] analyzing module s_adder
INFO: [VRFC 10-2263] Analyzing Verilog file "D:/fpga_projects/adder/src/adder_tb.v" into library work
INFO: [VRFC 10-311] analyzing module adder_tb

D:\fpga_projects\adder\sim>xelab -debug typical -top adder_tb -snapshot adder_tb_snapshot
```

```
D:\fpga_projects\adder\sim>xelab -debug typical -top adder_tb -snapshot adder_tb_snapshot

                            ilinx, Inc. All Rights Reserved.
                            /bin/unwrapped/win64.o/xelab.exe -debug typical -top adder_tb
-snapshot adder_tb_snapshot
Starting static elaboration
Pass Through NonSizing Optimizer
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module work.s_adder
Compiling module work.adder_tb
Built simulation snapshot adder_tb_snapshot

D:\fpga_projects\adder\sim>
```

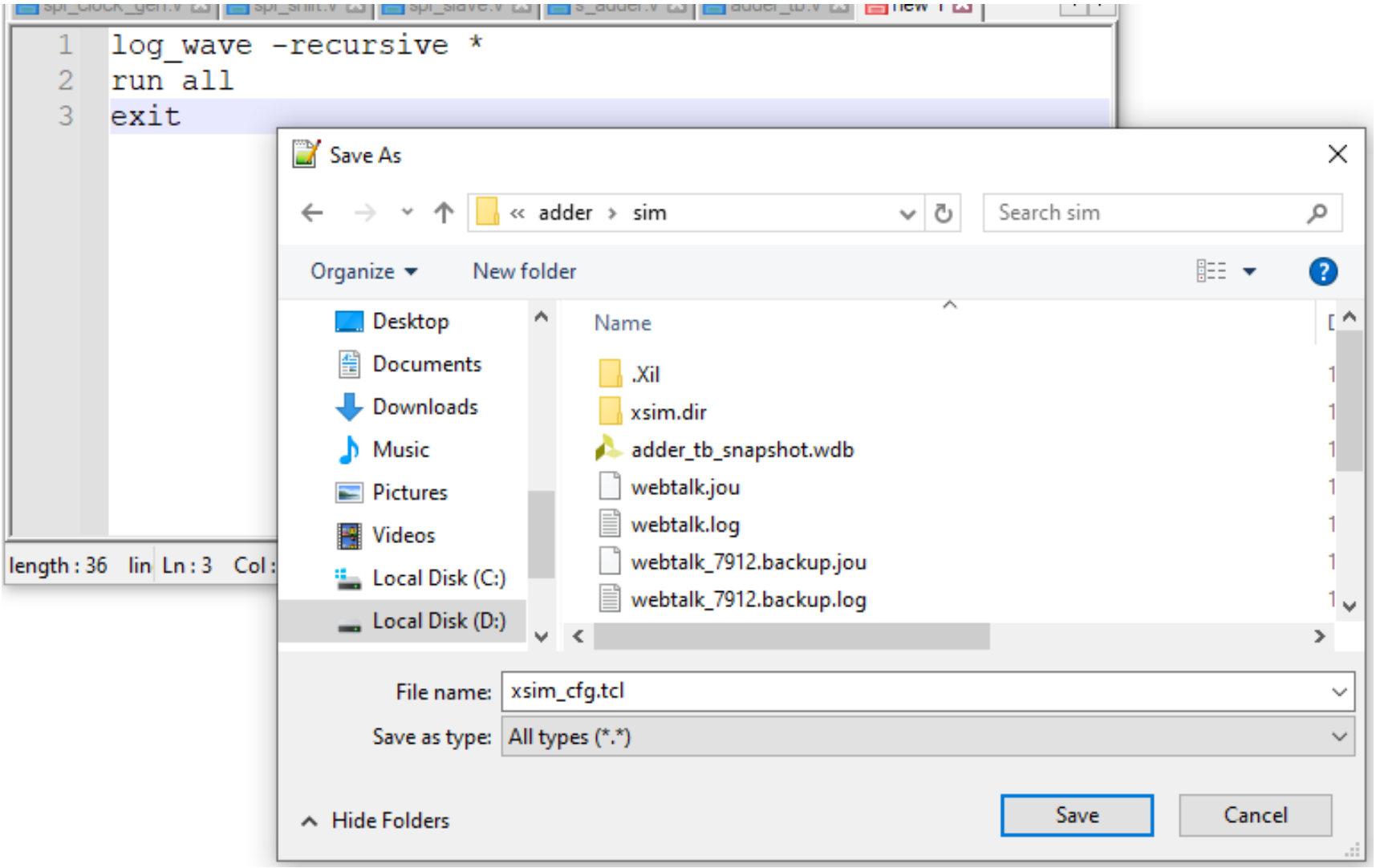
Simulation

```
D:\fpga_projects\adder\sim>xsim adder_tb_snapshot -R
```

-R in command promt ⇔ run all in GUI TCL shell

```
D:\fpga_projects\adder\sim>xsim adder_tb_snapshot -R

source xsim.dir/adder_tb_snapshot/xsim_script.tcl
# xsim {adder_tb_snapshot} -autoloadwcfg -runall

Time resolution is 1 ps
run -all
Time: 0 | a: 00000000000000000000000000000000, b: 00000000000000000000000000000000, sum: 00000000000000000000000000000000
Time: 10000 | a: 00000000000000000000000000000001, b: 00000000000000000000000000000001, sum: 00000000000000000000000000000010
Time: 20000 | a: 00000000000000000000000000000010, b: 00000000000000000000000000000001, sum: 00000000000000000000000000000011
Time: 30000 | a: 00000000000000000000000000000011, b: 00000000000000000000000000000011, sum: 00000000000000000000000000000110
$finish called at time : 40 ns : File "D:/fpga_projects/adder/src/adder_tb.v" Line 23
exit
INFO: [Common 17-206] Exiting xsim

D:\fpga_projects\adder\sim>
```

Waveform


1 log_wave -recursive *
2 run all
3 exit
length : 36 lin Ln : 3 Col :
Save As
« adder › sim
Search sim
Organize
New folder
Desktop
Documents
Downloads
Music
Pictures
Videos
Local Disk (C:)
Local Disk (D:)
Name
.Xil
xsim.dir
adder_tb_snapshot.wdb
webtalk.jou
webtalk.log
webtalk_7912.backup.jou
webtalk_7912.backup.log
File name: xsim_cfg.tcl
Save as type: All types (*.*)
Hide Folders
Save
Cancel

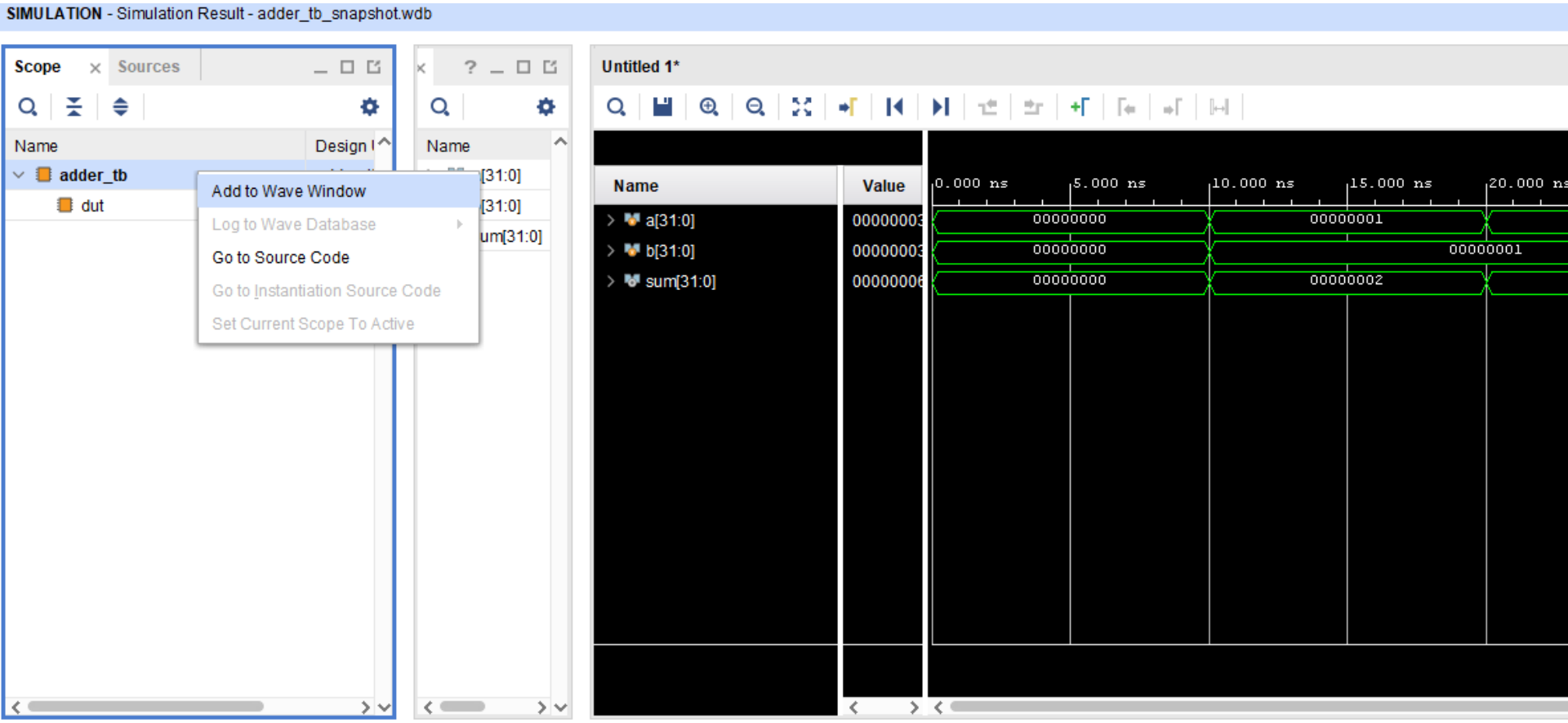
Waveform (2)

```
D:\fpga_projects\adder\sim>xsim adder_tb_snapshot --tclbatch xsim_cfg.tcl
```

```
D:\fpga_projects\adder\sim>xsim adder_tb_snapshot --tclbatch xsim_cfg.tcl




source xsim.dir/adder_tb_snapshot/xsim_script.tcl
# xsim {adder tb snapshot} -autoloadwcfg -tclbatch {xsim_cfg.tcl}

Time resolution is 1 ps
source xsim_cfg.tcl
## log_wave -recursive *
## run all
Time: 0 | a: 00000000000000000000000000000000, b: 00000000000000000000000000000000, sum: 00000000000000000000000000000000
Time: 10000 | a: 00000000000000000000000000000001, b: 00000000000000000000000000000001, sum: 00000000000000000000000000000010
Time: 20000 | a: 00000000000000000000000000000010, b: 00000000000000000000000000000001, sum: 00000000000000000000000000000011
Time: 30000 | a: 00000000000000000000000000000011, b: 00000000000000000000000000000011, sum: 00000000000000000000000000000110
$finish called at time : 40 ns : File "D:/fpga_projects/adder/src/adder_tb.v" Line 23
## exit
```

Waveform (3)

```
D:\fpga_projects\adder\sim>xsim --gui adder_tb_snapshot.wdb
```



Thank You