Design of mixed signal SOCs

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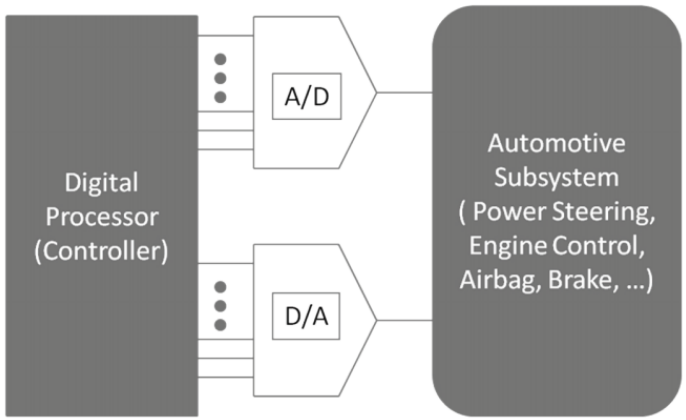
- Challenges
- Problems & Solutions
- Mixed signals and FPGAs

What is a mixed signal SOC?

- SOC with analog and digital signals
  - Measure analog signals and process right away
  - Create analog signals after processing digital input
  - Combination of both

- Examples:
  - Zybo
  - MSP430
  - Radio Modules
  - …



Example for a mixed-signal automotive design

Where is it used?

- Smart sensors
- IoT-Devices
- Small robots
- Software-defined Radio

Challenges

- High level of abstraction for IP and reuse based methodologies.
- Low level analysis for physical effects on small process nodes.
- Analog and digital IO, as well as RF integrated into one chip.

Problems

1. Simulation
   - Digital simulation does not support analog values
   - Analog circuit simulation too slow

2. Verification

3. Creating the chip
   - Electric Interference
   - RF behavior

Simulation: Real Number Models

- Digital simulation with real numbers
- Best used for high-frequency signals
- Low-frequency and DC simulation in SPICE
- Good simulation performance
- Example:
  - SystemVerilog (IEEE 1800-2012, SV-RNM)

Simulation: Verilog-AMS

- Analog behavioural modelling
- Works with standard digital test environments
- Continuous time analog simulation
- Analog and digital solvers

- Alternatives:
  - VHDL-AMS
  - SystemC-AMS

Simulation: Verilog-AMS Examples

- “electrical” adds voltage and current to pin-
- Contribution statement <+ assigns values continuously
- Instantiate modules between nodes and set values

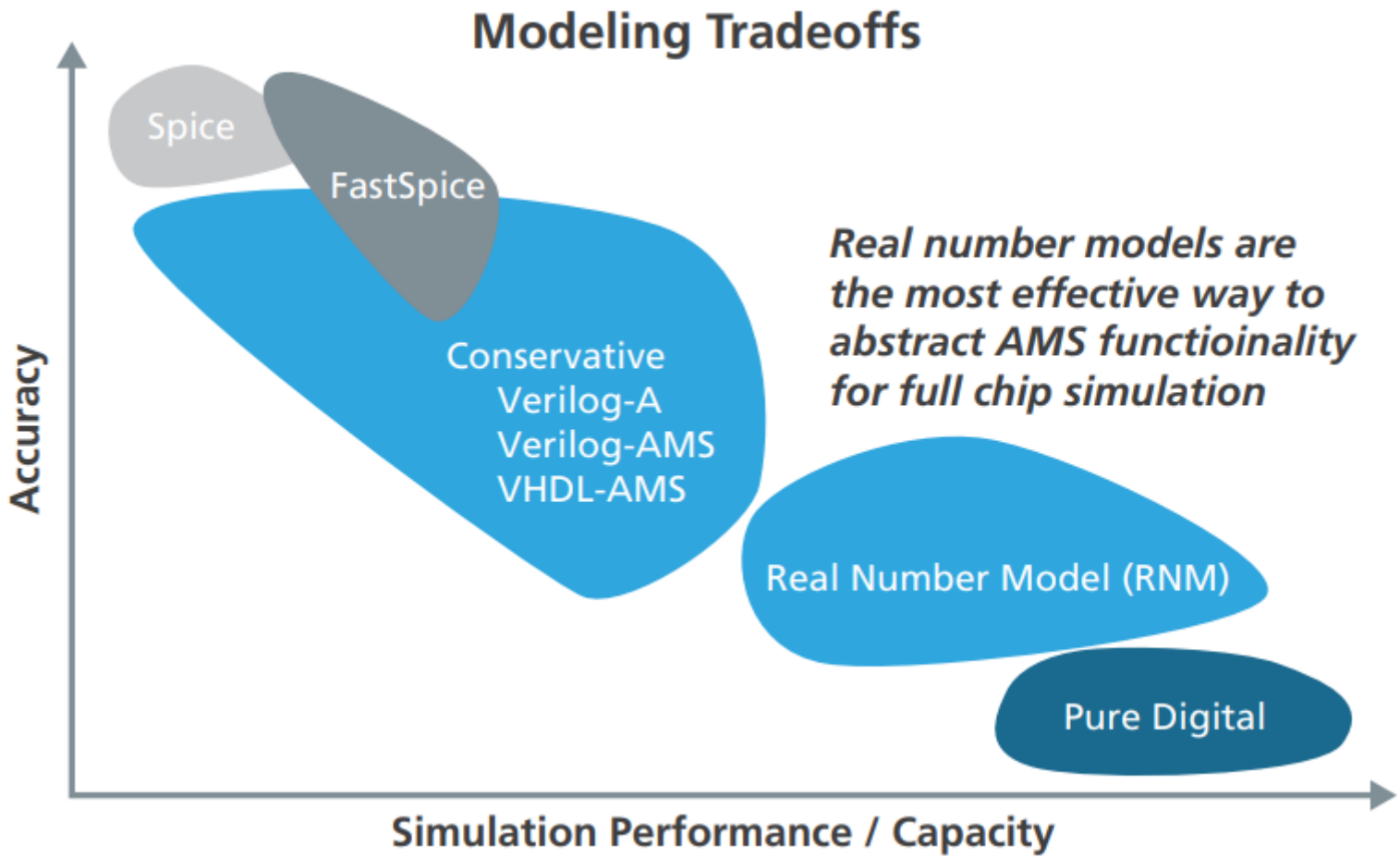
```
L1 (i1 0) inductor l=1uH
L2 (i2 0) inductor l=2uH r=1
```

```
module inductor(p, n);

  inout p, n;
  electrical p, n;
  parameter real l=1 from [0:inf);
  parameter real r=0 from [0:inf);

  analog begin
      V(p,n) <+ l*ddt(I(p,n)) + r*I(p,n);
  end
endmodule
```

Comparison of simulation methods



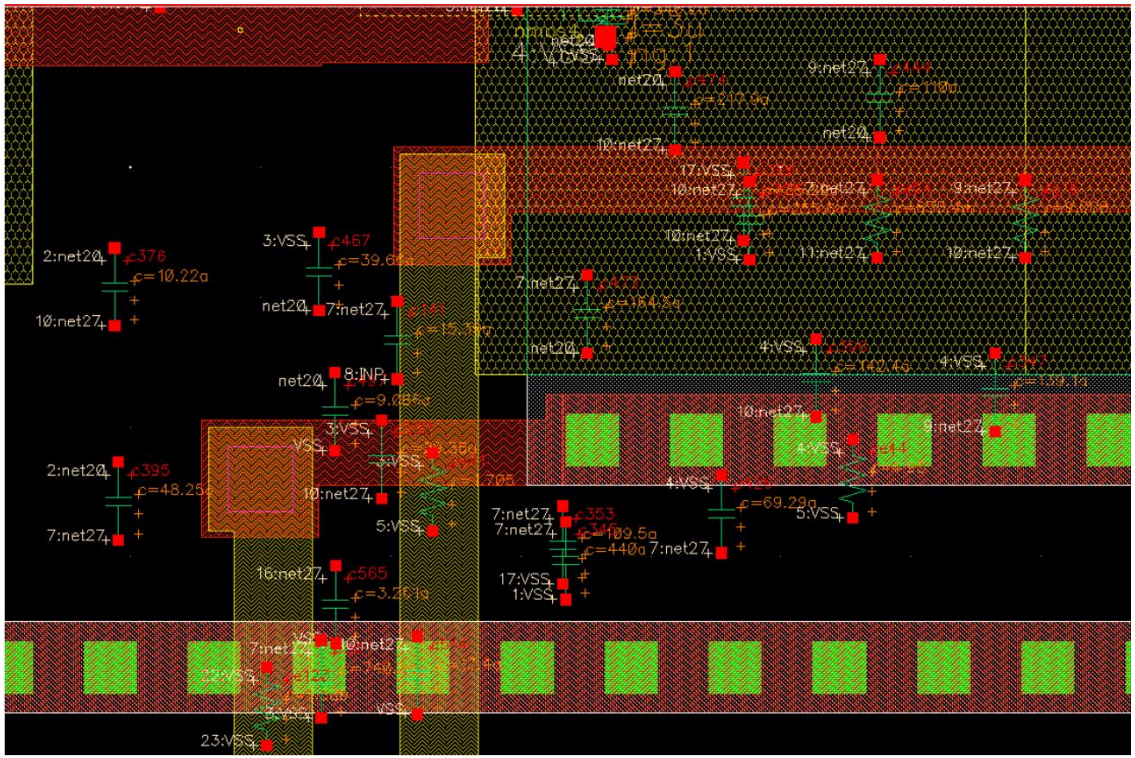
Verification

- Digital verification:
  - Universal Verification Methodology (UVM)
  - Metric-driven Verification (MDV, Coverage driven)

- Mixed-Signal Verification:
  - MS-MDV
  - UVM with RNM
  - Allows assertions with real numbers
  - Requires well-tested individual blocks

Parasitic extraction

- Large parasitic effects for small processes
- Post layout simulation

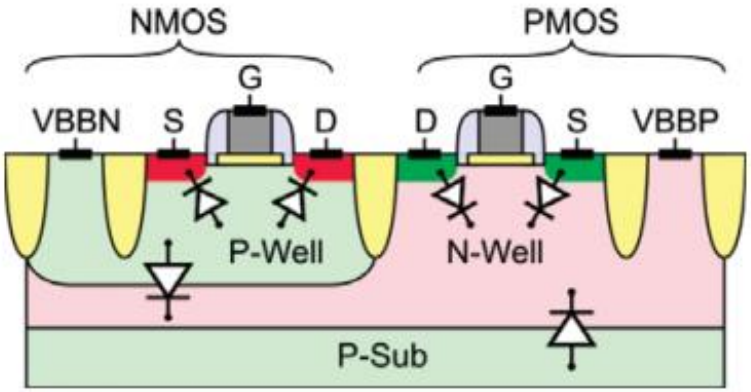


Verification

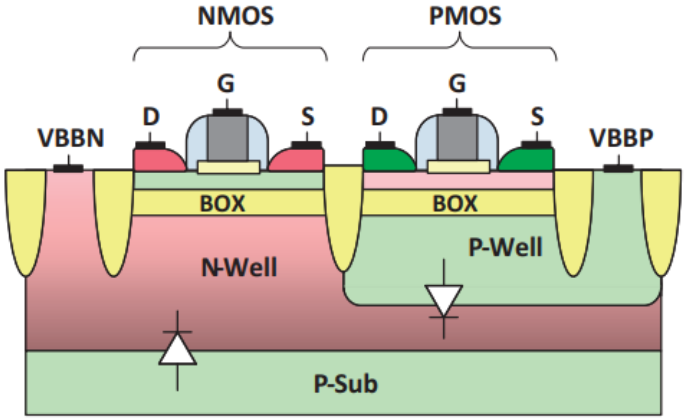
- Time to market, first time right
- Simulation performance
- Shrinking process nodes => physical effects
- Interaction between analog and digital

- Foundry verified golden models and simulators
- Tight link to parasitic extraction tool
- Support for multiple levels of circuit abstraction

Silicon on insulator



Traditional CMOS



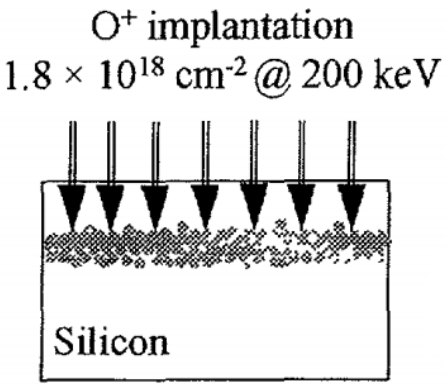
Silicon on insulator

- Parasitic diodes connected to the substrate
- Substrate coupling

Silicon on insulator

SIMOX: Separation by Implantation of Oxygen

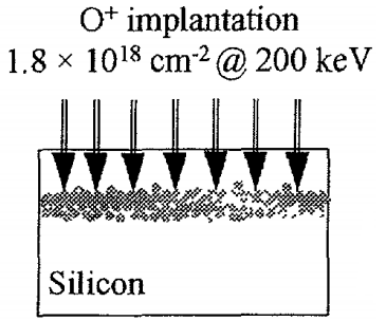
- Implant O^+ Ions, energy and fluence determines range and thickness
- Continuously anneal damaged silicon @ 600-1400°C



Silicon on insulator

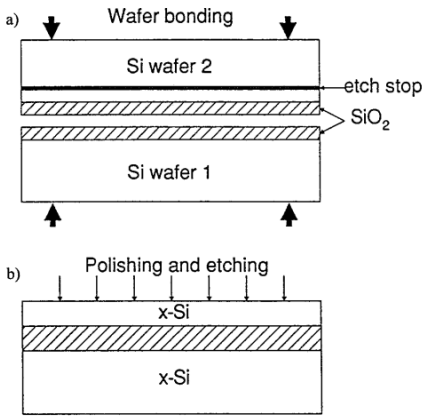
SIMOX: Seperation by Implantation of Oxygen

- Implant O^+ Ions, energy and fluence
- determines range and thickness
- Continuously anneal damaged silicon @ 600-1400°C



BESOI: Bond and Etch-Back SOI

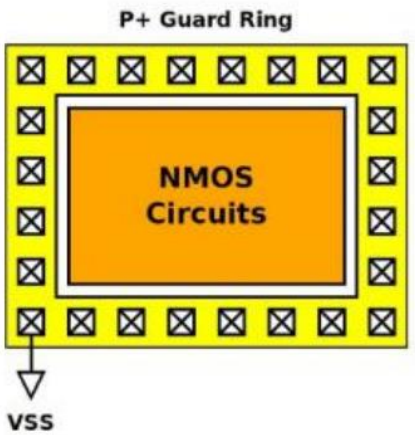
- Bond to separate wafers
- Create etch block by implanting B or Ge.



SOI vs Guard rings

Guard ring: Ring in silicon and metal layers

- Reduce substrate coupling significantly
- Increased area
- Easy



Silicon on Insulator

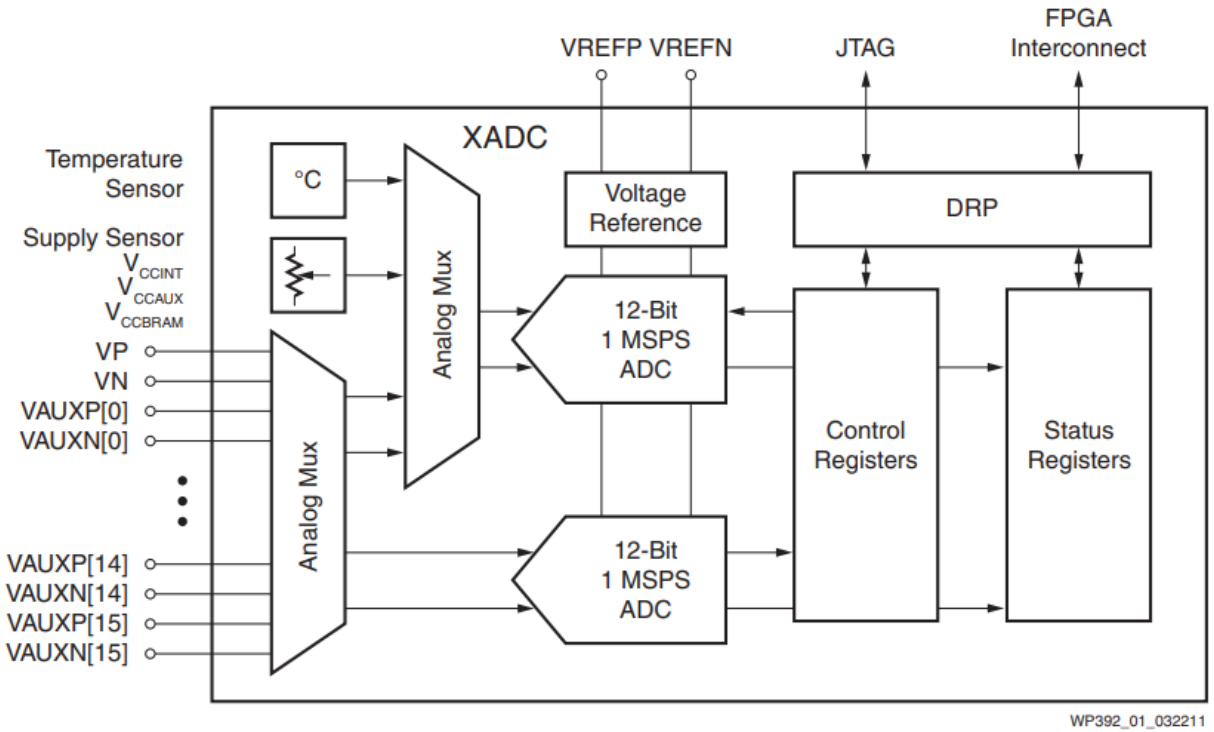
- Reduced substrate coupling
- Reduced gate and parasitic capacity
- No additional area
- More expensive

Mixed signals and FPGAs

- FPGAs support only digital signals
- Digital input from ADC, analog output by DAC
- Placed on the chip or provided by processor
- System is mixed-signal, FPGA is not
- Prototype FPAAs, nothing useful yet

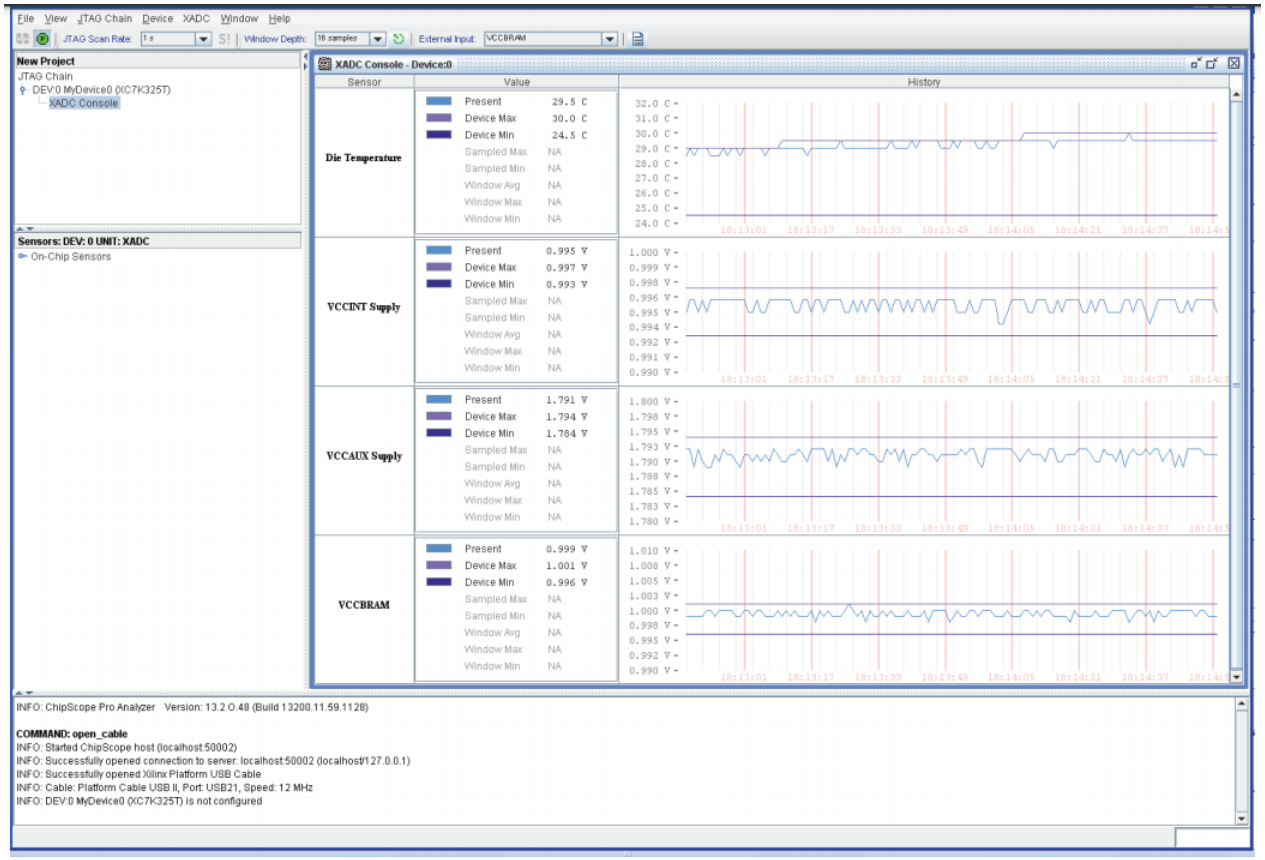
Zynq-7000

Internal dual 12 bit ADC with 1Msps



ChipScope Pro

View analog Inputs without design



Sources

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