Summary of GUI Testbench

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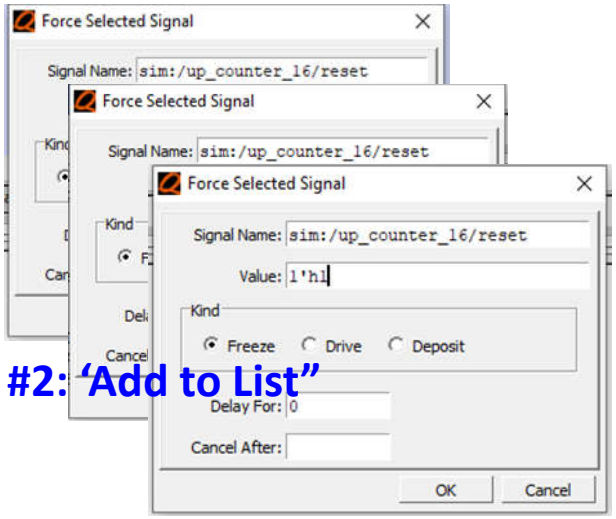
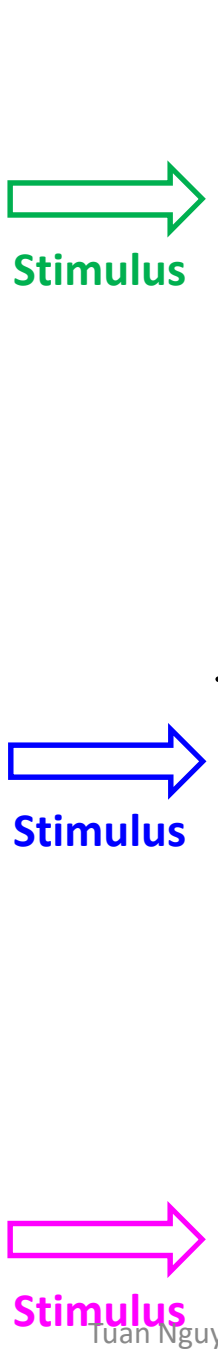
```
always #5 clk = ~clk;

initial
    begin
        // 1. Initialize testbench variables to 0
        clk <= 0;
        rstn <= 0;
        // 2. Drive rest of the stimulus
        #20 rstn <= 1;
        #80 rstn <= 0;
        #50 rstn <= 1;
        // 3. Finish the stimulus after 200ns
        #20 $finish;
    end
```

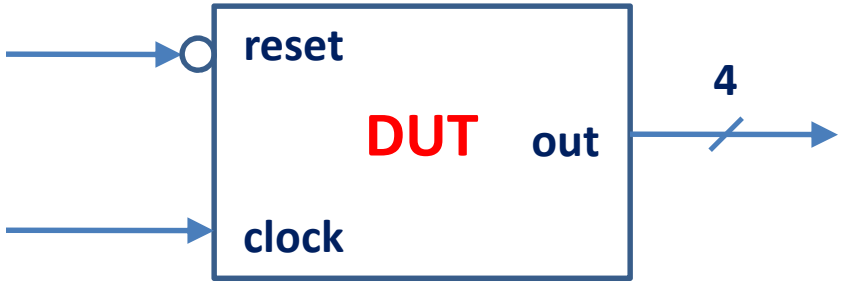
#1: Verilog testbench file



#2: 'Add to List"

#3: writing .DO file





Thank You